جامعة الملك عبدالله
للعلوم والتقنية
King Abdullah University of
Science and Technology

IEEE EDS Distinguished Lecture 20th June 2013
IEEE Central Texas Section
ED/CEDA/CAS/SSC Joint June Meeting

Integrated Nanotechnology for Sustainable Future and Smart Living

Dr. Muhammad Mustafa Hussain
Assistant Professor, Electrical Engineering
Integrated Nanotechnology Lab @ KAUST

Living in digital age – a social technology

60 HOURS OF VIDEO

6,000 SONGS

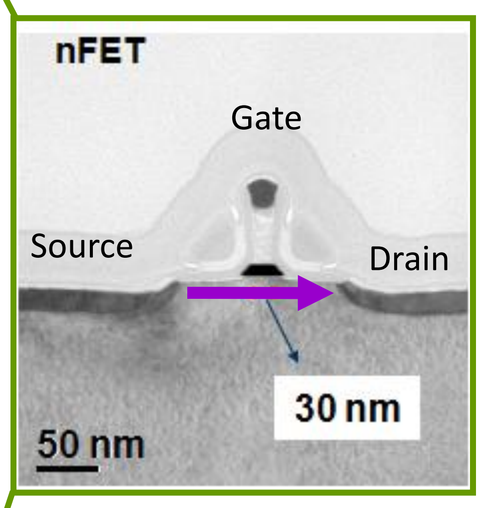
170,000 PHOTOS

230,000 TWEETS

204,000,000 E-MAILS

7 EXABYTES OF DATA/DAY

8 EXABYTES IN 2015

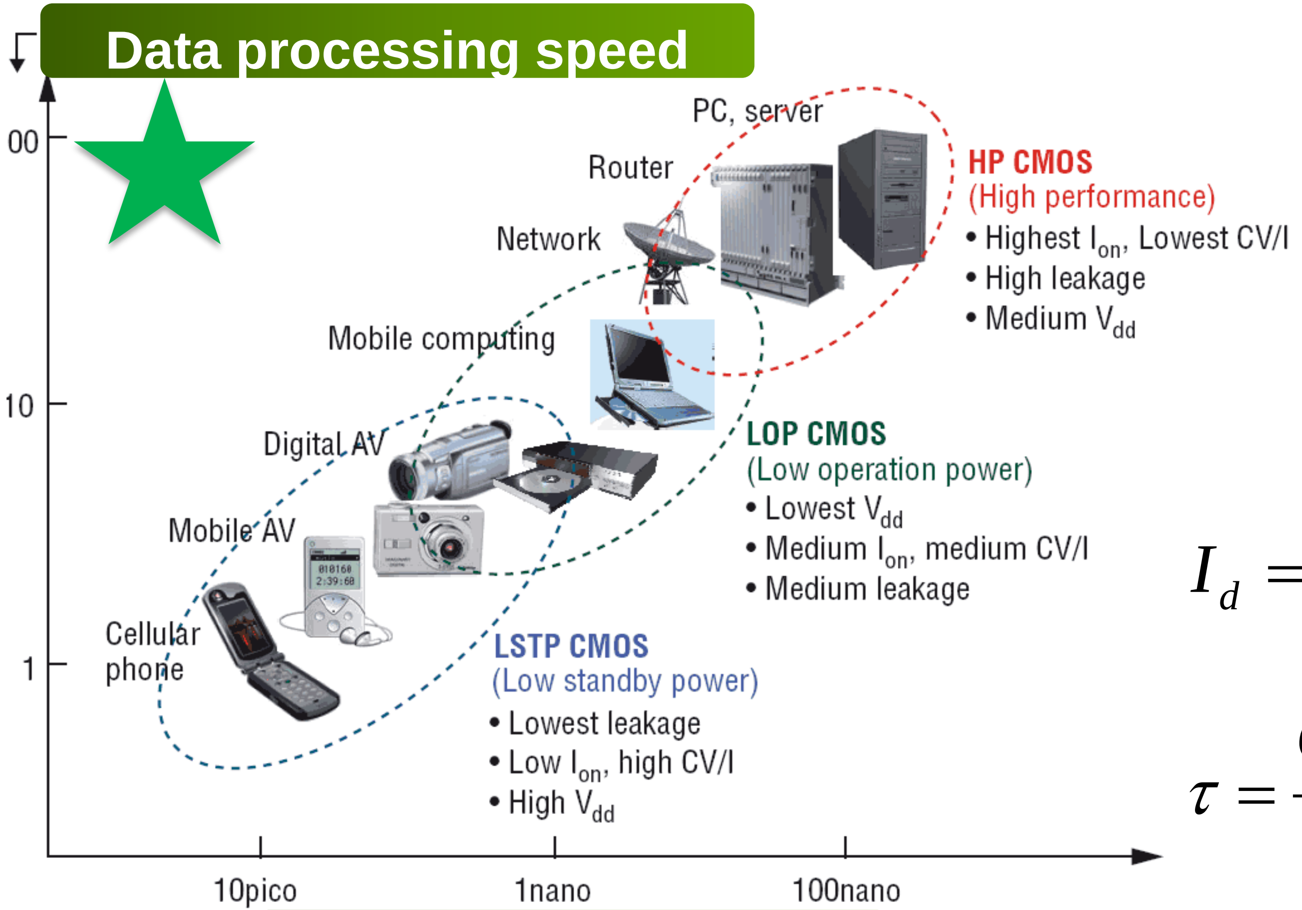


M. M. Hussain 2008

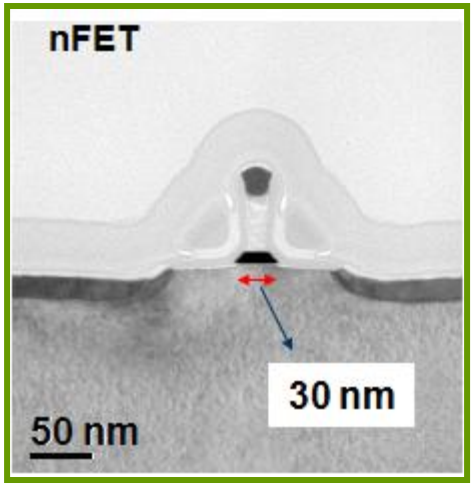
Deeply integrated into our daily life – a social technology

Evolution “was” and “is” not easy

Data processing speed



Less battery lifetime



$$I_d = \frac{W}{l_g} C_{ox}\mu(V_g - V_t)$$

$$\tau = \frac{C_g V_{dd}}{I_d}$$

$$P_{off} = V_{dd} W_{Total} I_d$$

Major change in 3 decades …

Controlled by the designers

Increase mobility

Minimized for power saving

$$I_d^{sat} \approx \mu C \frac{W}{L}(V_g - V_t)^2$$

Very low ~ 0.3V

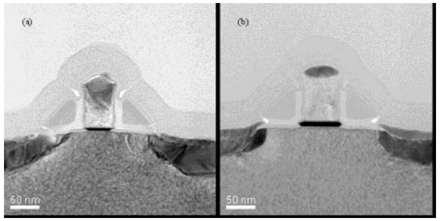
Use high-k

$$C = \frac{\kappa}{t_{dielectric}}$$

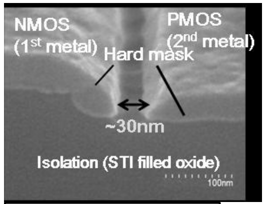
Scale $t_{dielectric}$

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	Faster transistor
Leakage	>100x reduction	Cooler chips

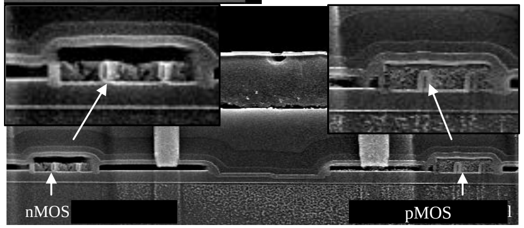
TECHNOLOGY INSERTION POINTS
INTEL HIGH-K/METAL GATE 2008
INTEL TRI-GATE FET 2011



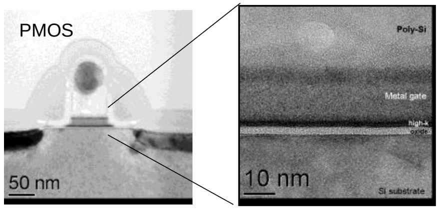
Dual metal gate/high-k Planar CMOS (MM Hussain et. al. VLSI 2005)
[Si, HfO_2, Ru, TaSiN]



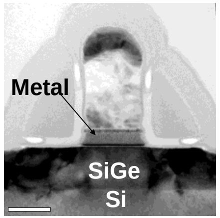
Dual high-k/ dual metal gate CMOS (MM Hussain et. al. VLSI 2006)
[Si, HfO_2, Al_2O_3, TaSiN, TiN]



Dual metal gate FinFET CMOS (MM Hussain et. al. ESSDERC 2007, TED 2010)
[Si, HfSiON, TiN]

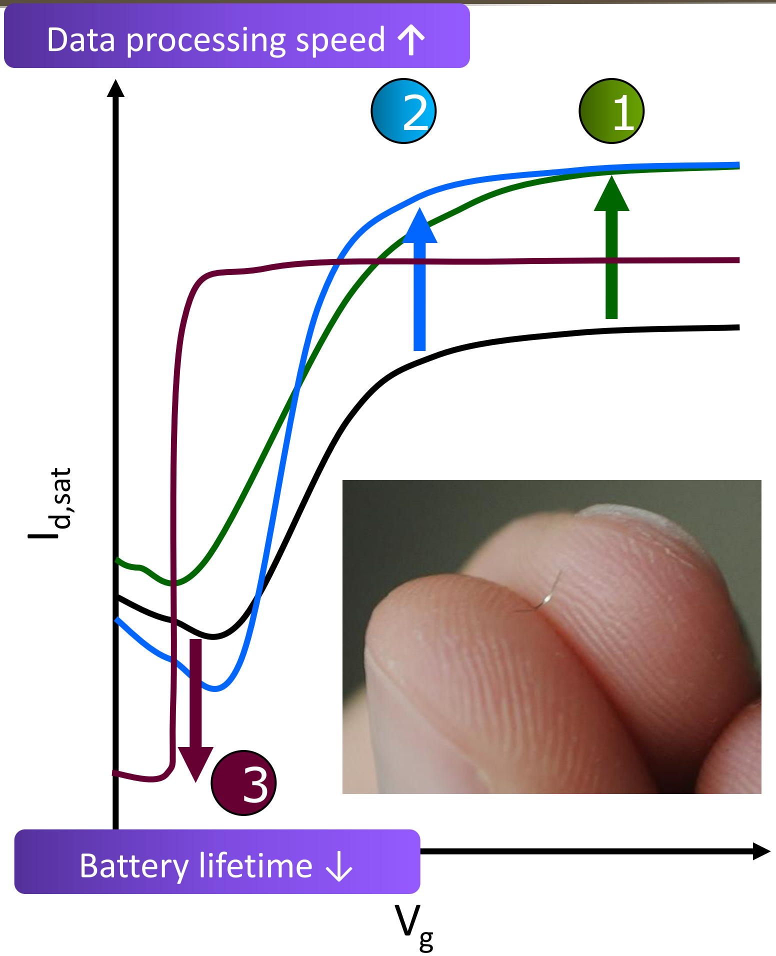


Single metal/single high-k CMOS (MM Hussain et. al. VLSI 2009)
[Si, HfSiON, La_2O_3, Al_2O_3, TiN]

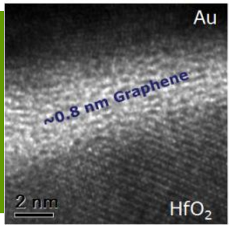


Dual channel single metal/single high-k CMOS (MM Hussain et. al. TVLSI 2010, ISTDM 2010)
[Si, SiGe, HfSiON, La_2O_3, TiN]

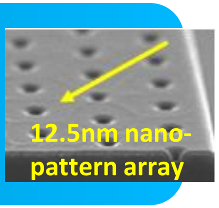
Jumping up and down …



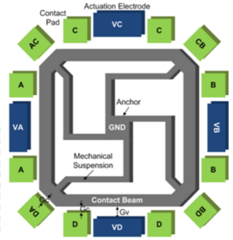
High mobility channel material:
Si (alloyed), traditional II-IV and III-V
2D atomic crystal structure materials



Better electrostatic control:
Non-carbon Nanotube FET
High density nanowire circuit integration



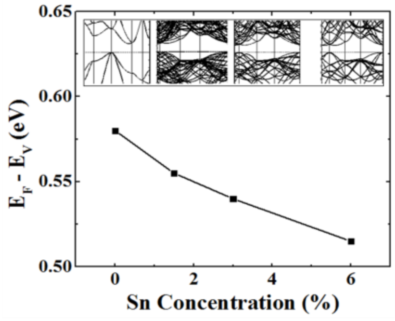
Improved I_{on}/I_{off} ratio:
Ultra low power multi-states electro-mechanical switch for parallel data processing

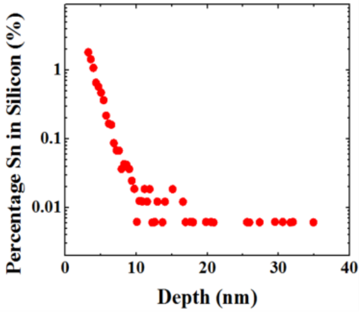


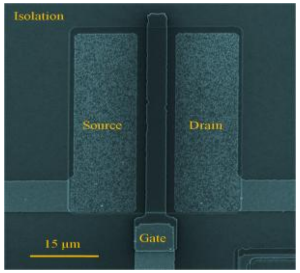
High thermal budget compatible, reusable, flexible Si (100)

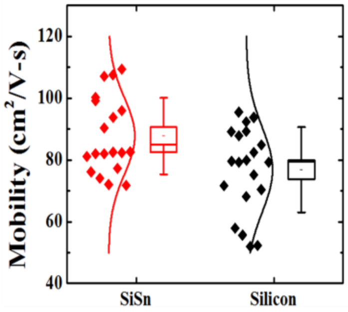
Pushing Moore’s Law @ KAUST

- Tin (Sn) – an unlikely ally of silicon for enhanced performance in transistor (AM Hussain et. al. IEEE TED, DRC 2013) [in collaboration with Dr. N. Singh and Prof. Schwingenschloegl]

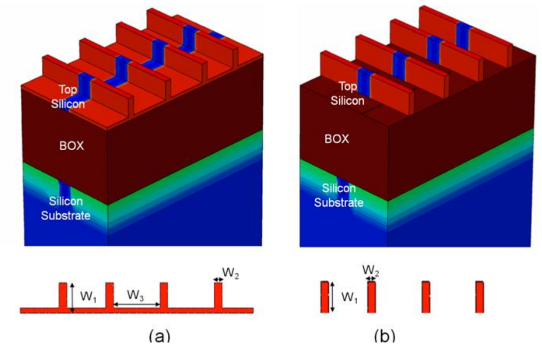


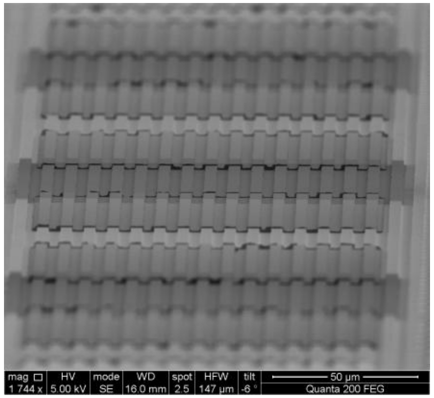


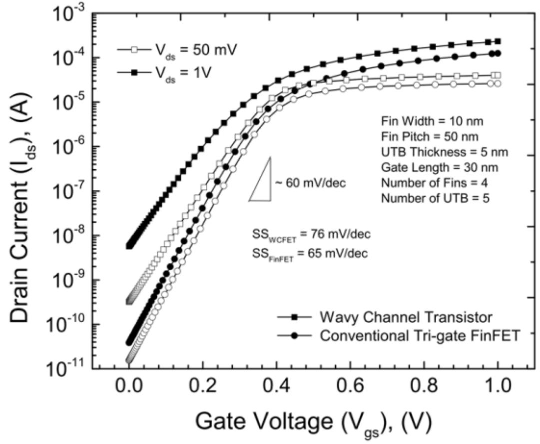




- Wavy channel transistor to enhance performance of FinFET and thin film transistors (material irrespective) (HM Fahad et. al. APL 2013)





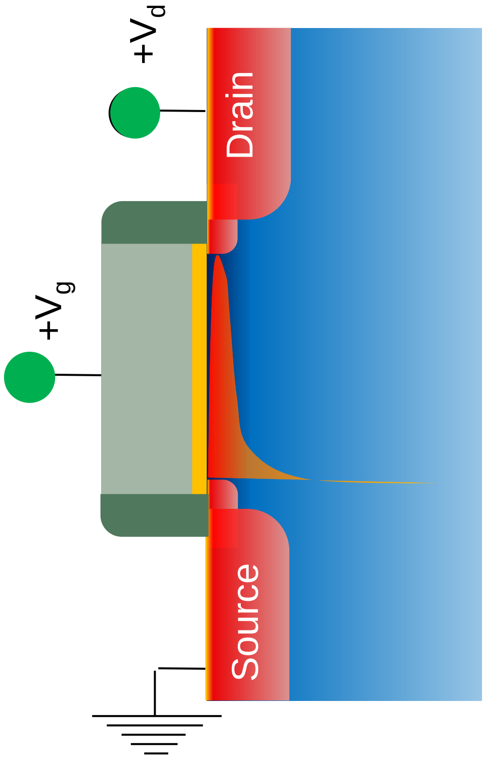


Information – anywhere, anytime

Touch screen – sensors
Communication and multimedia – electronics
Navigation – MEMS

Every person will have a handheld portable device which has:
High performance computation capability
Longer battery lifetime
High resolution display
Conveniently powered
Easily deployable and affordable

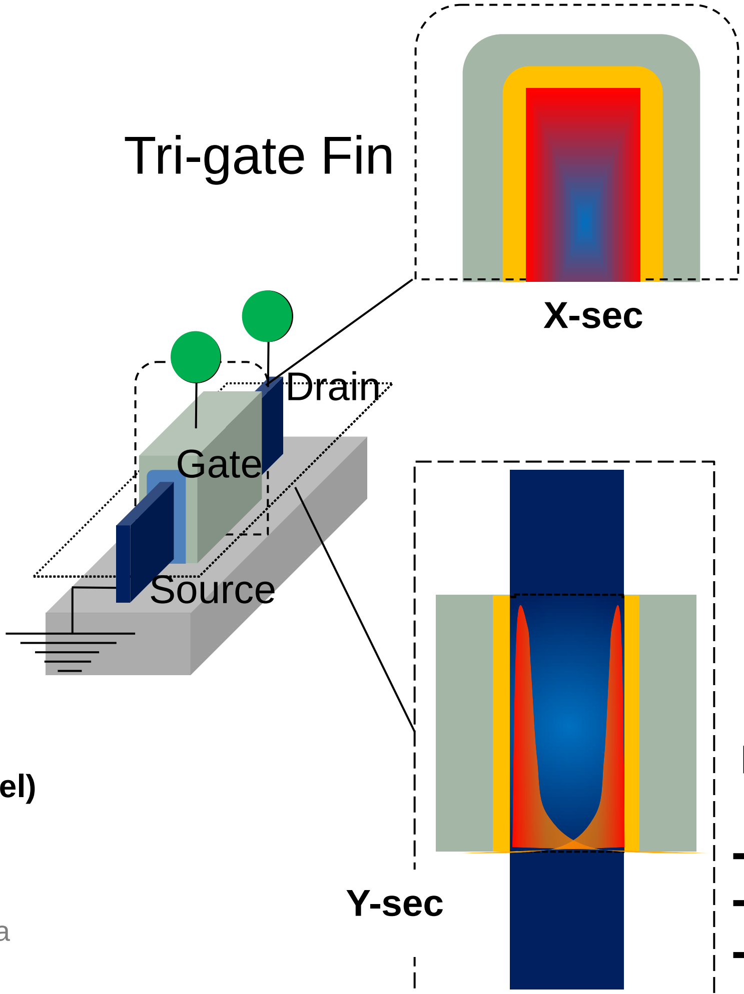
Evolution of modern transistors



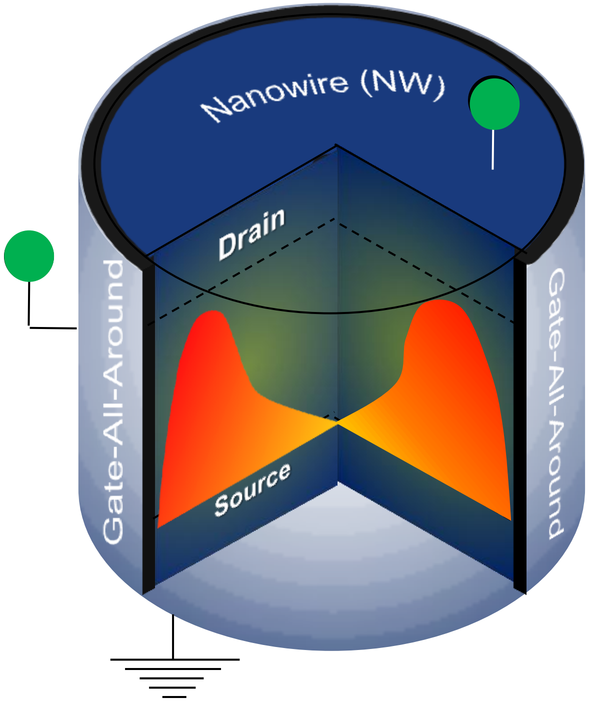
2D sheet of charges (channel) in a Gaussian Profile

Classical MOSFET

3D sheet of charges (in the channel) creating multiple Gaussian Profile Volume inverted channel


Tri-gate Fin

Gate all around nanowire FET



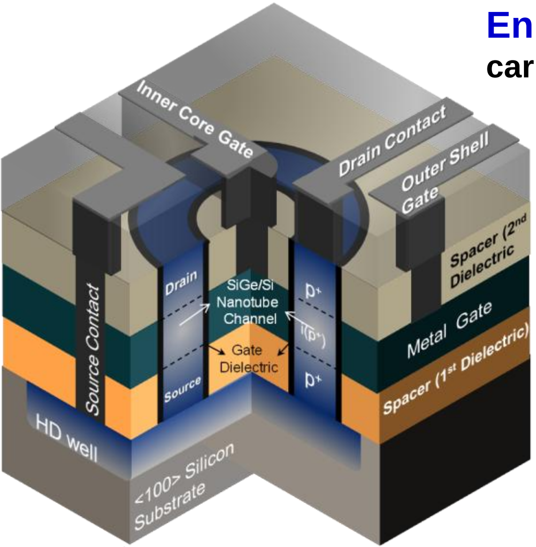
Multiple gates

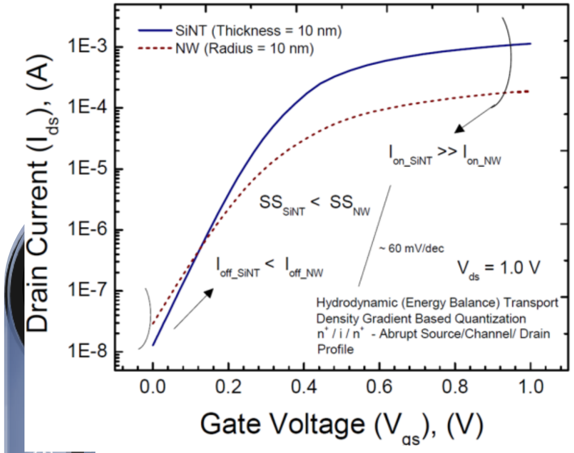
- → Better electrostatics
- → Improved leakage
- → Reduced short channel effects

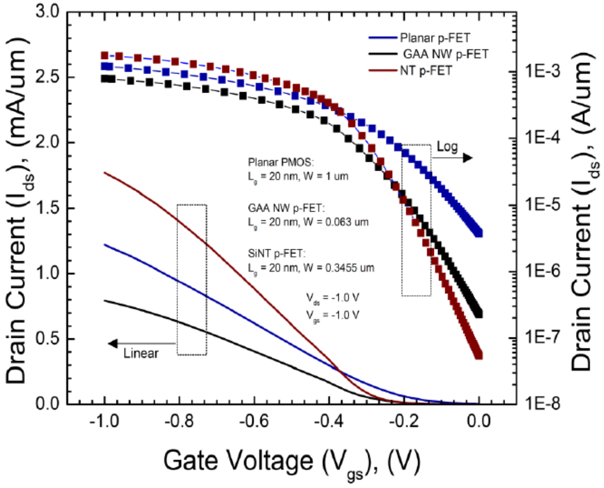
New architecture to play with new physics

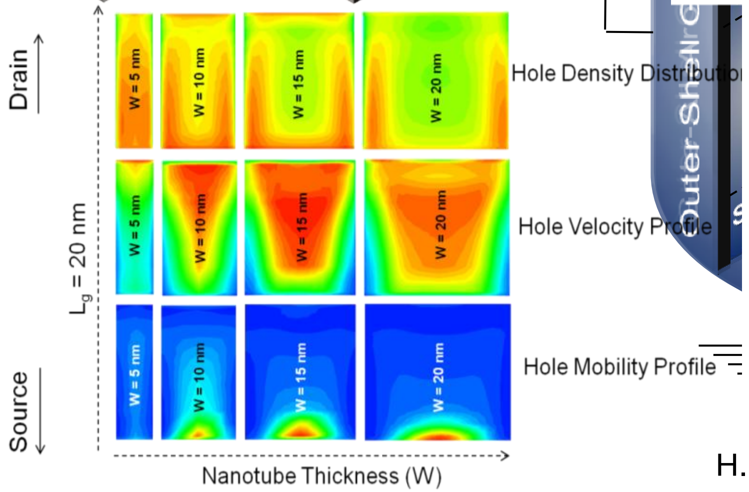
Ultimate hybrid high performance and low power FET

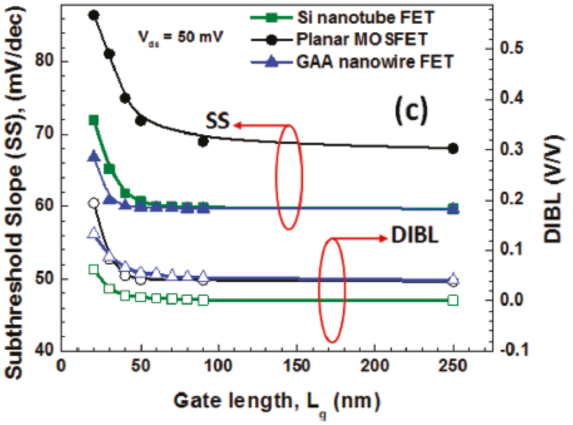
Enhanced I_{on} due to more volume inverted carriers to flow through compared to nanowires.







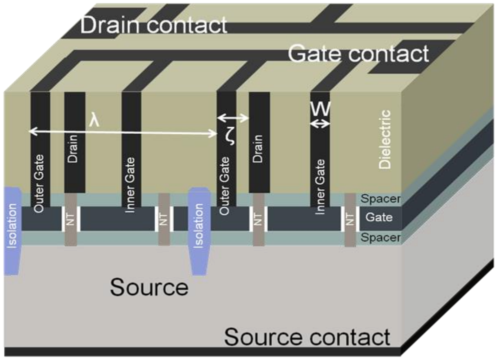




Reduced (Comparable) leakage (I_{off}), DIBL, SS compared to ultra-thin (sub-20 nm) nanowires.

H. M. Fahad and M. M. Hussain Scientific Report, Nature Publishing Group (2012)

Nanotube or nanowire?

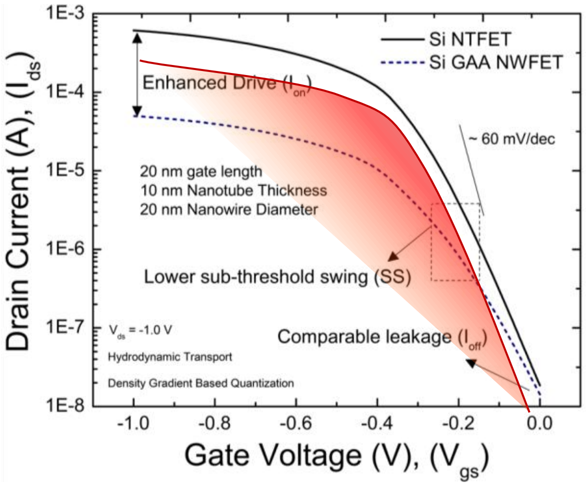


2 x Vertically stacked NTFET

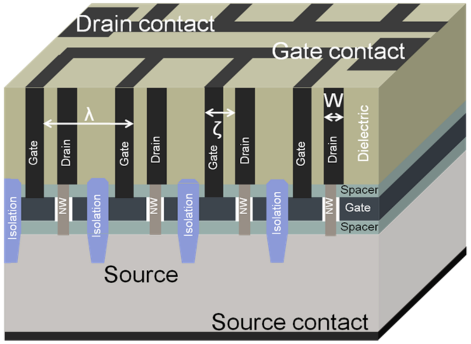
$$A_{NT} = 1 \times (\lambda + \zeta + 3 \times W)$$

$$S_{NT} \propto (A_{NT})^{-3/2} \propto {}^{1}/(RC)_{NT}$$

$$P_{NT} \propto CV^2$$



1 x Nanotube (HP red zone) = 13 x Nanowires



4 x Vertically stacked GAA NWFET

$$A_{13NW} = 13 \times (\lambda + \zeta + 2 \times W)$$

$$S_{13NW} \propto (A_{13NW})^{-3/2} \propto {}^{1}/(RC)_{13NW}$$

$$P_{13NW} \propto CV^2$$

Consequences of NW arraying:

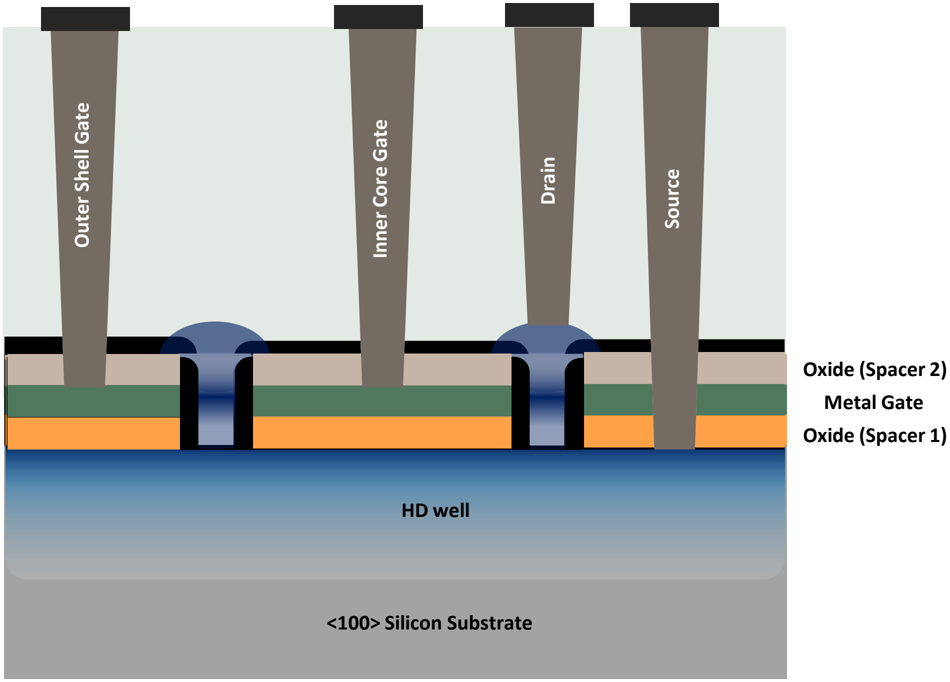
1. Large chip area consumption
2. Reduced chip speeds (increased RC delays)
3. Increased Power consumption
4. Increased off-state leakage
5. Increased SCE

Benefits of a single NT over an array of 13 NWs

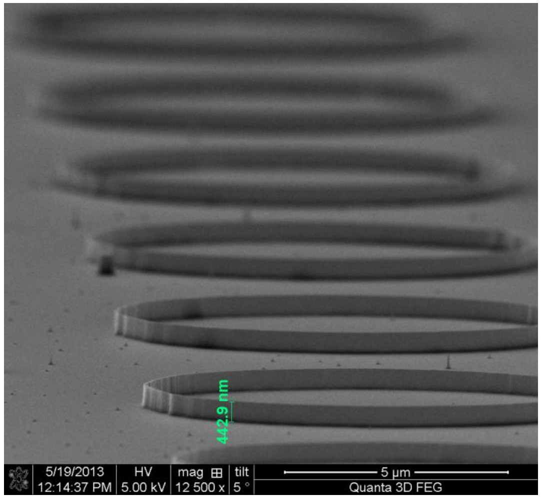
Area Advantage	Speed Advantage	Power Advantage
A_{13NW}/A_{NT}	S_{NT}/S_{13NW}	P_{13NW}/P_{NT}
91%	**37x**	**97.3%**

M. M. Hussain, H. M. Fahad, R. Qaisi Invited feature article physica solidi status (a) (2012)
H. M. Fahad, M. M. Hussain – IEEE Trans. Elect. Dev. March 2013

Large scale integration of nanotube and nanowire FET



- Deposit oxide/metal/oxide gate stack
- Pattern and etch through stack (NT definition)
- Conformal gate dielectric (spacer) deposition
- Directional spacer/dielectric etch
- Selective silicon epitaxy in patterned trenches
- Deposit inter layer dielectric (ILD)
- Etch contact holes
- Contact hole metal fill
- Deposit and pattern contact electrodes

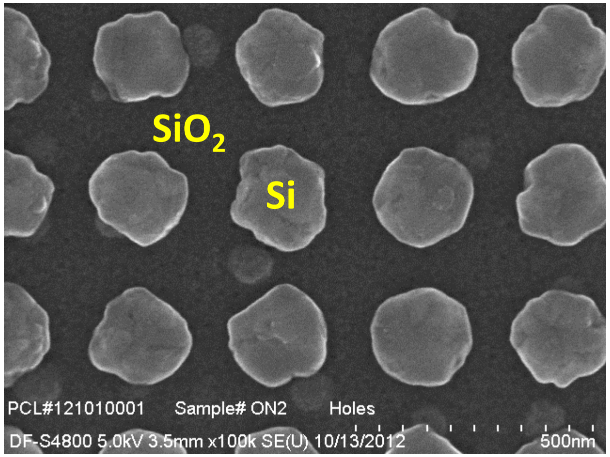


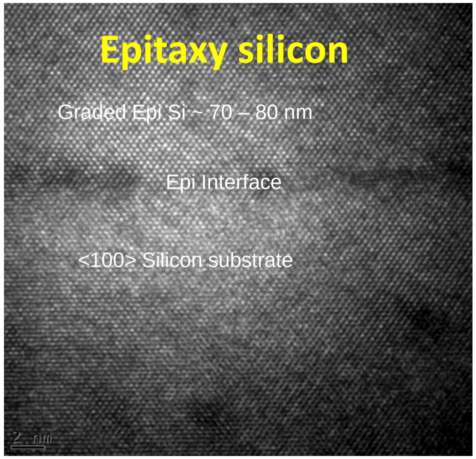
Advantages,

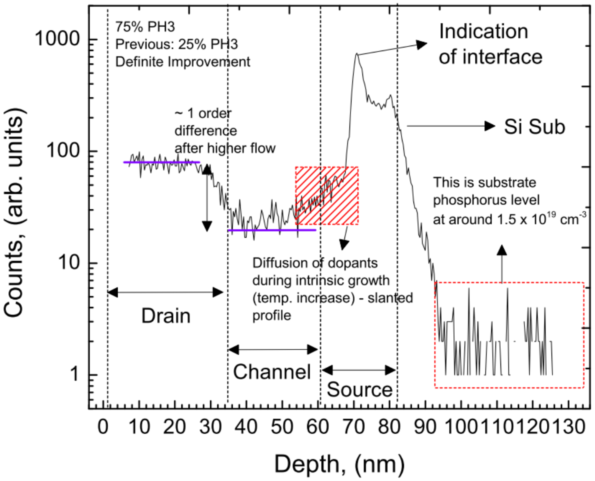
1. Deposition controlled gate length (L_g) definition
2. Precise nanotube alignement and arraying possible
3. In-situ doping for steep source/channel and drain/channel junctions:
   - Ballistic performance enabler
   - Mitigated RDFs in nanotube channel
   - Ability to use other epi-based channel materials

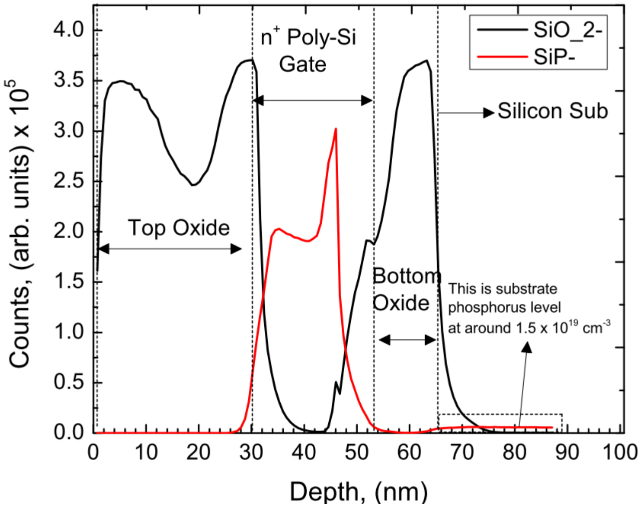
J. P. Rojas, M. M. Hussain (IEEE NANO 2012) and H. M. Fahad, M. M. Hussain (MRS Fall 2012)

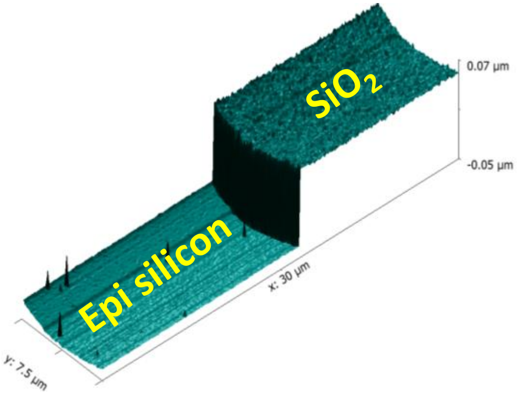
Physical analysis of process developments

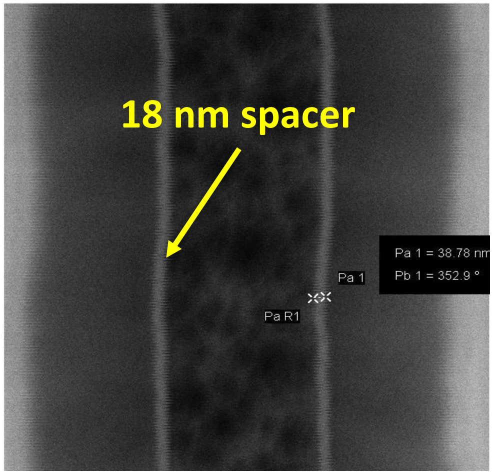






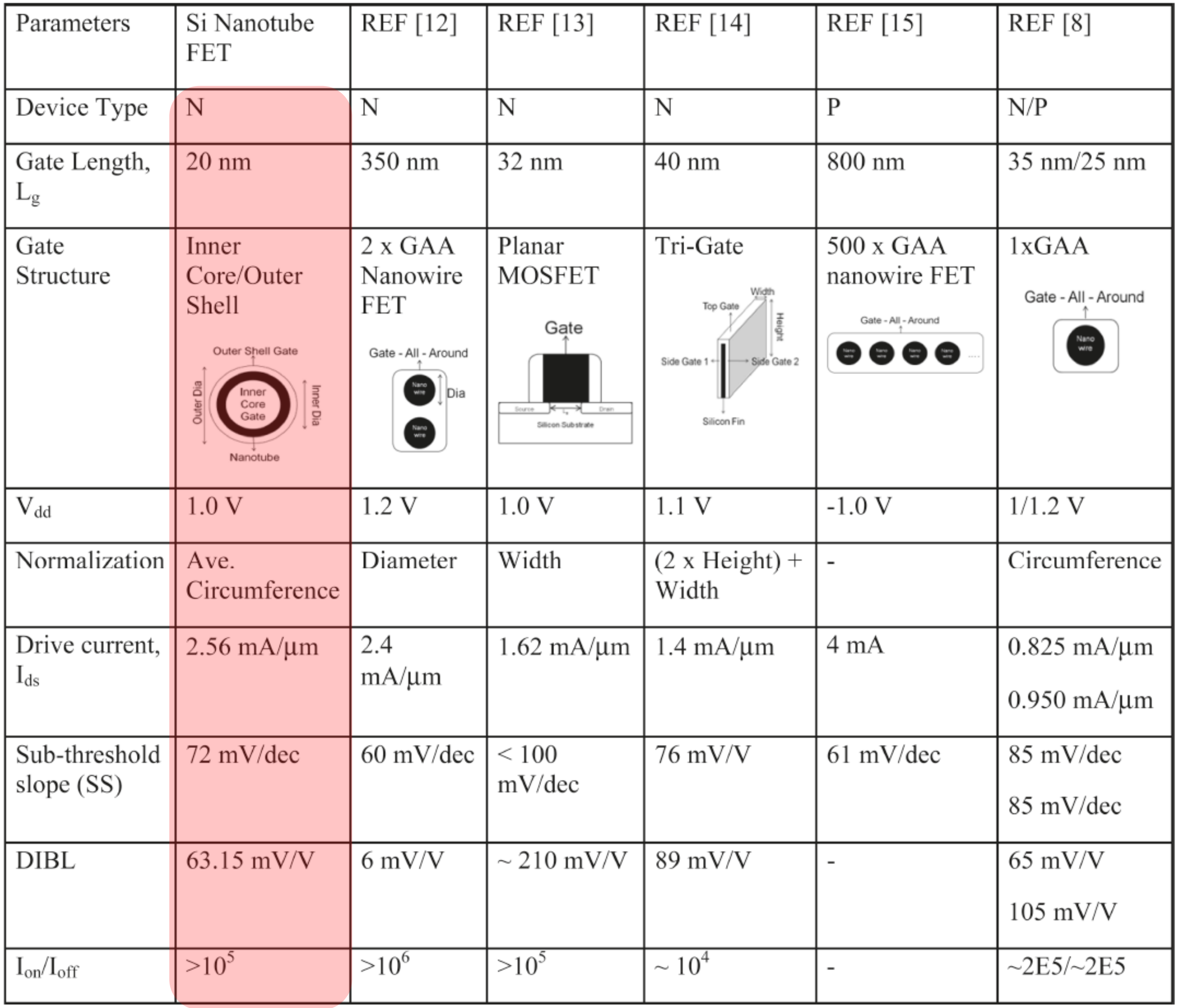






Benchmarking with other reports

Single Nanotube FET device without arraying stands out of the crowd

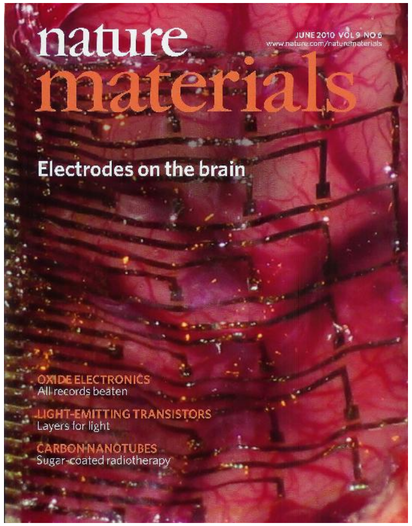


Parameters	Si Nanotube FET	REF [12]	REF [13]	REF [14]	REF [15]	REF [8]
Device Type	N	N	N	N	P	N/P
Gate Length, L_g	20 nm	350 nm	32 nm	40 nm	800 nm	35 nm/25 nm
Gate Structure	Inner Core/Outer Shell	2 x GAA Nanowire FET	Planar MOSFET	Tri-Gate	500 x GAA nanowire FET	1xGAA
V_{dd}	1.0 V	1.2 V	1.0 V	1.1 V	-1.0 V	1/1.2 V
Normalization	Ave. Circumference	Diameter	Width	(2 x Height) + Width	-	Circumference
Drive current, I_{ds}	2.56 mA/µm	2.4 mA/µm	1.62 mA/µm	1.4 mA/µm	4 mA	0.825 mA/µm 0.950 mA/µm
Sub-threshold slope (SS)	72 mV/dec	60 mV/dec	< 100 mV/dec	76 mV/V	61 mV/dec	85 mV/dec 85 mV/dec
DIBL	63.15 mV/V	6 mV/V	~ 210 mV/V	89 mV/V	-	65 mV/V 105 mV/V
I_{on}/I_{off}	$>10^5$	$>10^6$	$>10^5$	$\sim 10^4$	-	~2E5/~2E5

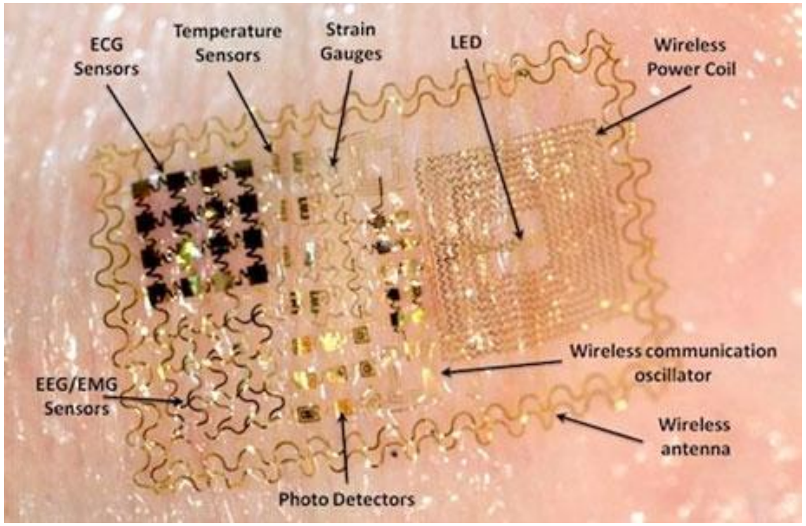
H. M. Fahad, C. E. Smith, J. P. Rojas, M. M. Hussain, Nano Letters 2012

Status quo in flexible electronics

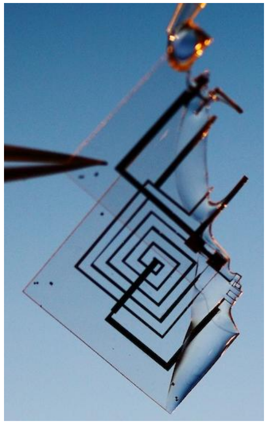
JA Rogers 2006



JA Rogers 2010

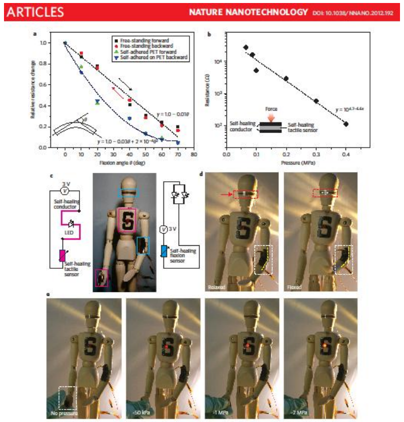


JA Rogers in Science 2011

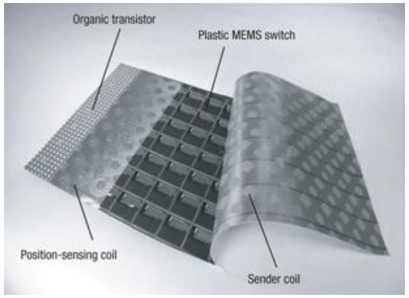


JA Rogers in Science 2012

JA Rogers in Nature 2013



Z Bao 2013



T Someya in Nat. Mat. 2007

Can we build a truly high performance computer which is flexible and transparent?

Display – available

SPEED 3.1 GHz 850M DEVICES Mobility 220 cm^2/V-s

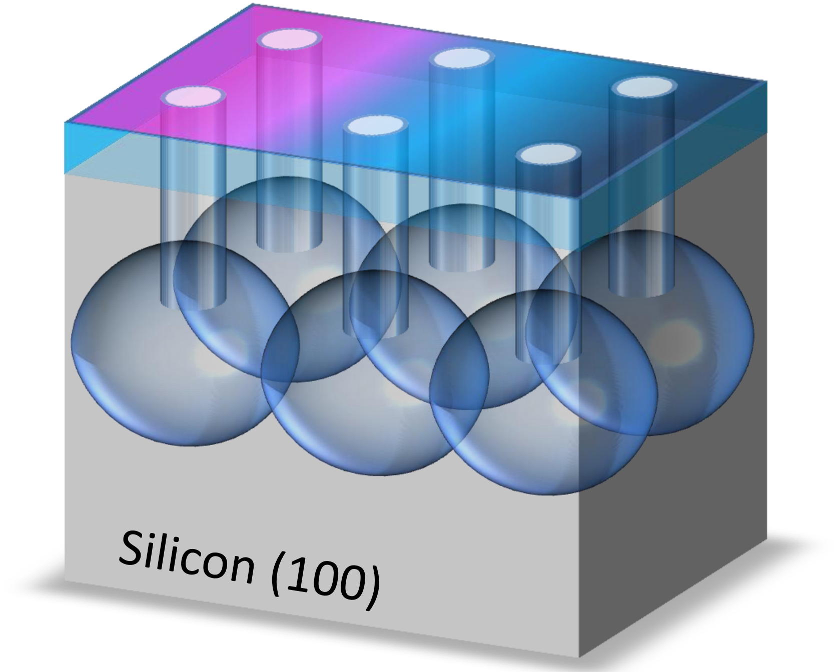
Method	Speed	Challenge
Organic	Extremely slow	Fundamentally slow
Back grinding	Good	Cost and damage
Exfoliation	Potentially very high	Uncertainty
Carrier technique	Good	Cost
Hybrid	Intel 286 processor	Size, cost, integration

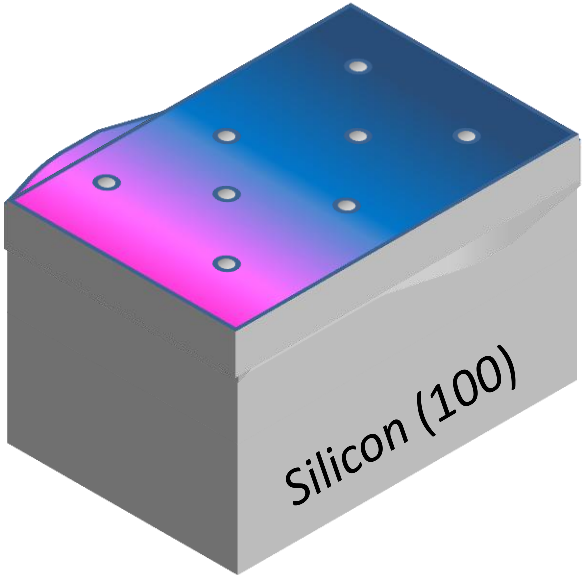
Needed:
1. Usage of bulk silicon (100)
2. Low-cost proven process technology
3. High-thermal budget compatibility
4. Recyclability

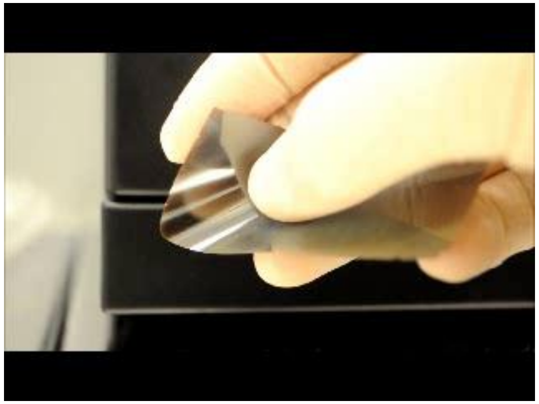
Our approach

- ❑ *“Trench-protect-release”*
- ❑ *Bulk mono-crystalline silicon (100)*
  - ❑ *Mobility*
  - ❑ *Cost*
- ❑ *High-k/metal gate stacks*
  - ❑ *Low power*
- ❑ *Standard CMOS compatible processes*
  - ❑ *High thermal budget*
  - ❑ *Integration density*
  - ❑ *Existing toolsets*
  - ❑ *Low cost processes – no epitaxy, no high energy ion implantation, no stressor, no back grinding, no ultra-thin commercially available silicon*
  - ❑ *Recyclability*

Generic process to transform traditional electronics into flexible and semi-transparent one …







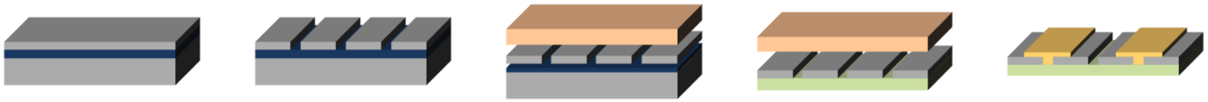
J. P. Rojas, A. Syed, M. M. Hussain (MEMS 2012)

Various approaches for flexible electronics

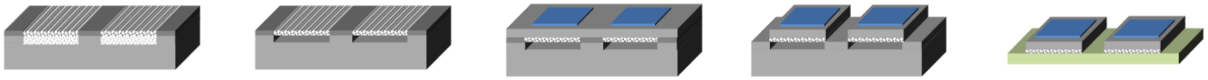
Organic/ CNT/NW/2D


Metal gate on polymer
Dielectric
Semiconductor composite
Patterning
Top contacts

Transfer Printing


Silicon-on-Insulator (SOI)
Implantation and Patterning
Micro/nano ribbons release
Transfer onto polymer substrate
Contacts

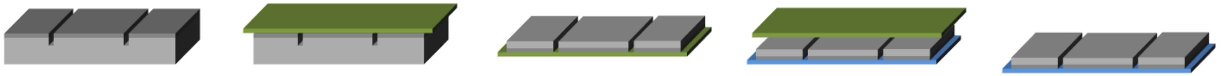
Chipfilm^{TM}


Implantation, 2 steps Si anodization (2 porous layers)
Hydrogen sintering (1100°C, 30 min)
Epitaxial Si overgrow, CMOS fabrication
Deep trenches for release
Transfer onto Polymer substrate

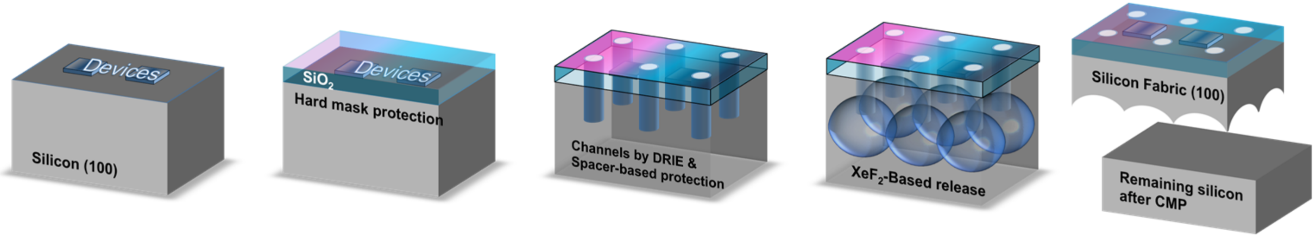
Spalling/ Exfoliation


CMOS fabrication
Stressor deposition
Fracture by stress mismatch
Transfer onto Polymer substrate
Stressor removal

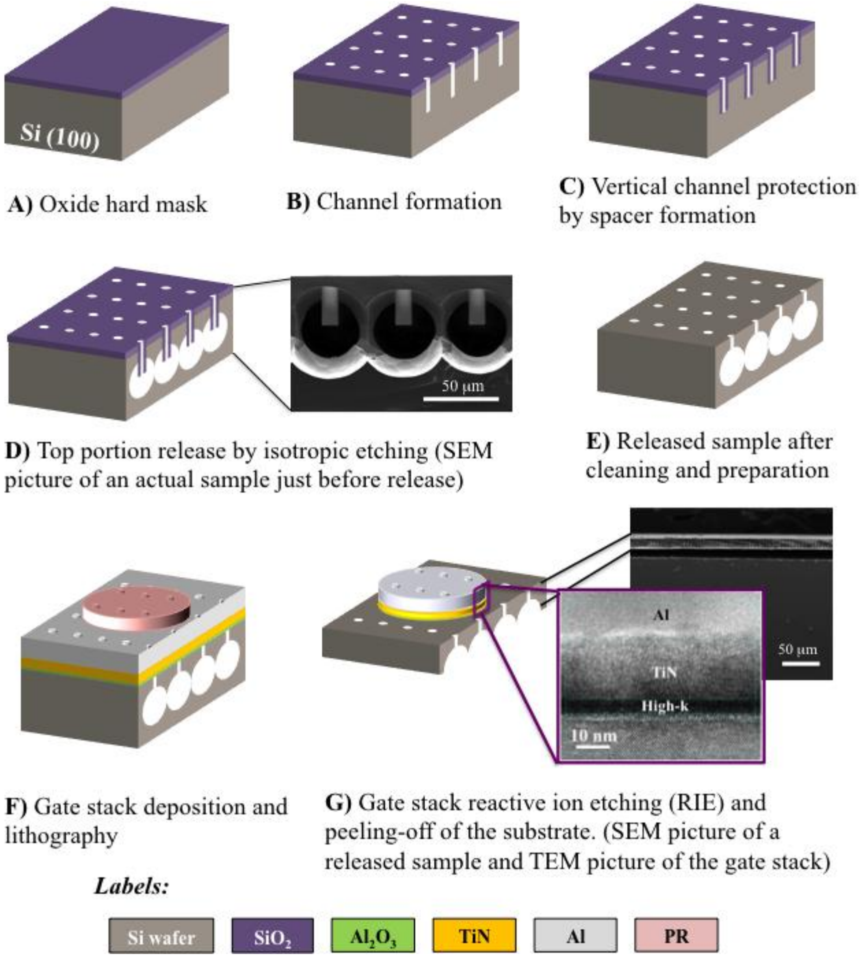
Back-grinding


CMOS fabrication And pre-cut/dicing
Tape for support
Grinding process
Transfer onto Polymer substrate

Flexible Si Fabric



High-κ/metal gate MOSCAPs – Device Last



A) Oxide hard mask

B) Channel formation

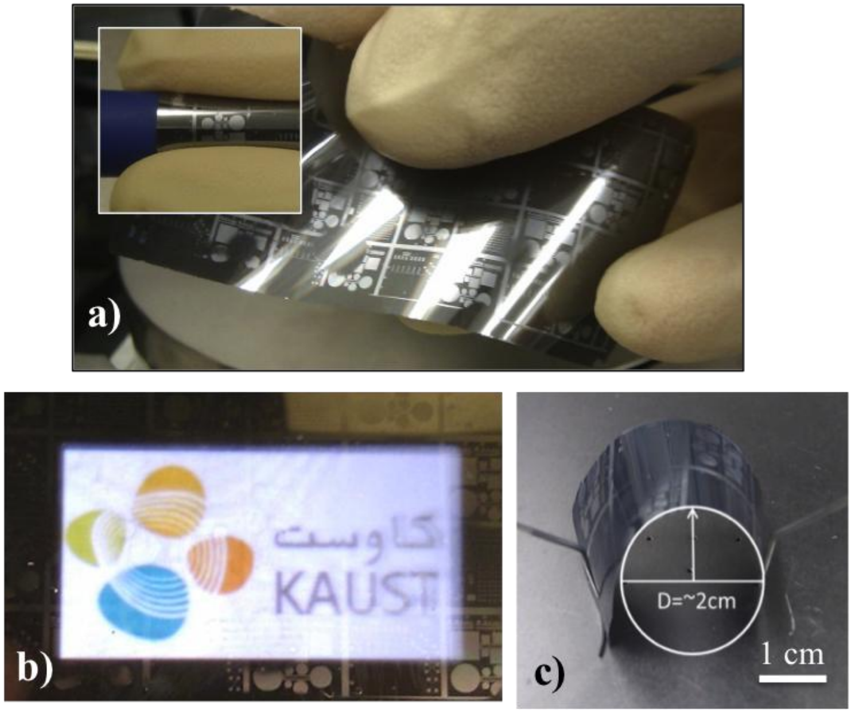
C) Vertical channel protection by spacer formation

D) Top portion release by isotropic etching (SEM picture of an actual sample just before release)

E) Released sample after cleaning and preparation

F) Gate stack deposition and lithography

G) Gate stack reactive ion etching (RIE) and peeling-off of the substrate. (SEM picture of a released sample and TEM picture of the gate stack)

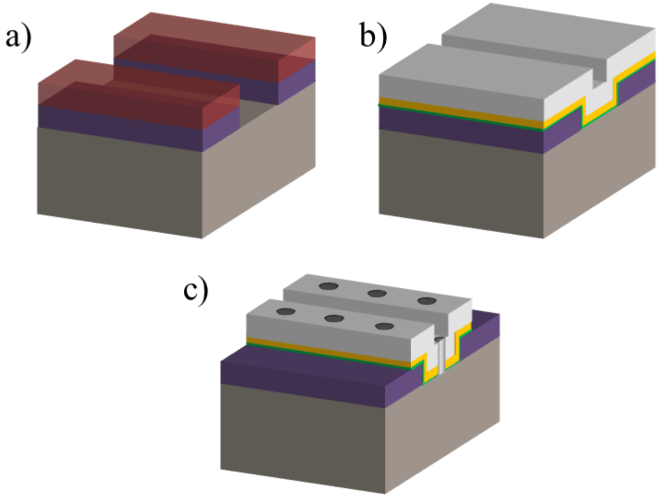


Device last is possible – after silicon release

J. P. Rojas, M. M. Hussain (pss-RRL 2013)

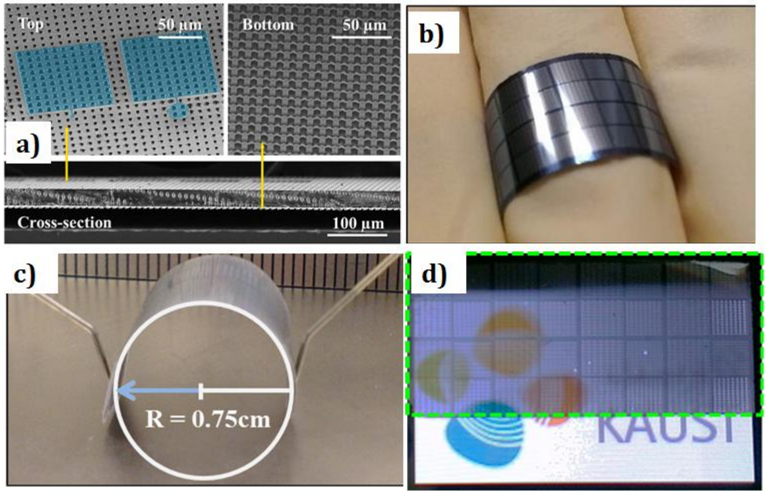
High-κ/metal gate MOSCAPs – Device First

***STAGE I*. MOSCAP fabrication**

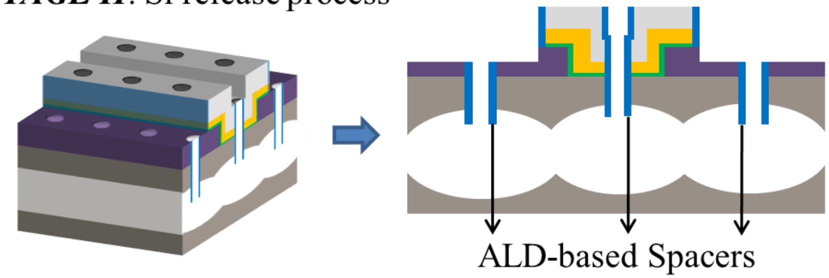


Labels:

- **Si wafer**
- **SiO_2**
- **Al_2O_3**
- **TaN**
- **Al**
- **PR**
- **AlO_X Spacers**



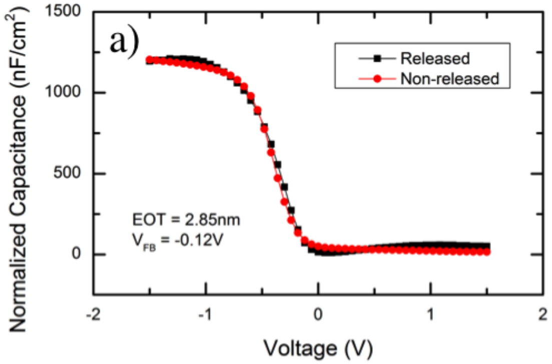
***STAGE II*. Si release process**

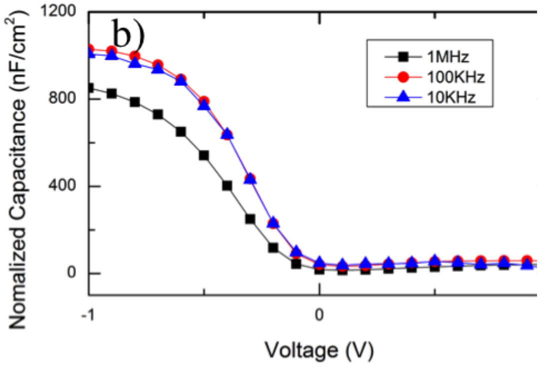


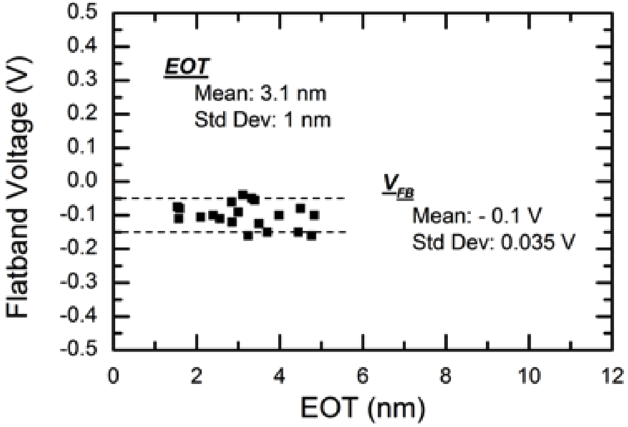
- ☐ ***Device first – before silicon release***
- ☐ ***Process compatibility via contact pad***

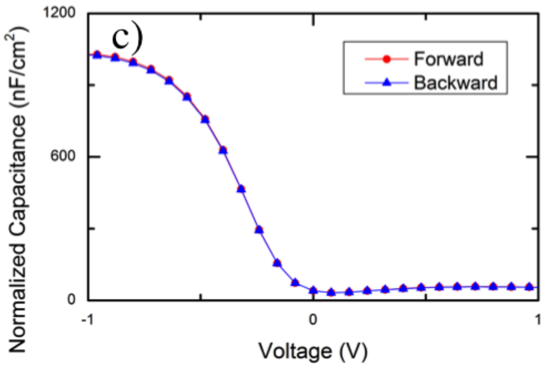
J. P. Rojas, G. A. Torres Sevilla M. M. Hussain (APL 2013)

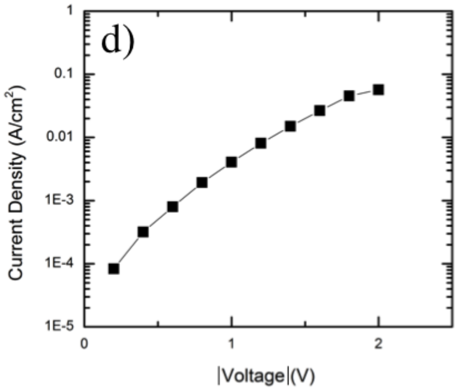
Ultra-low power consumption







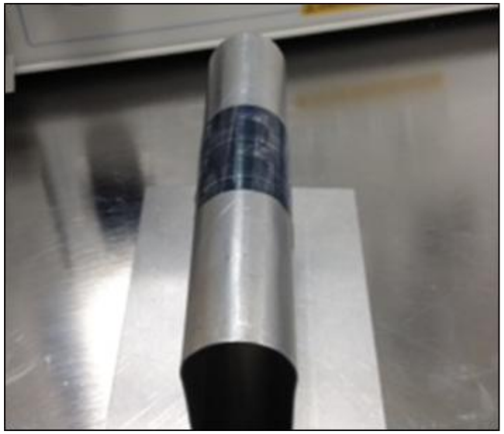


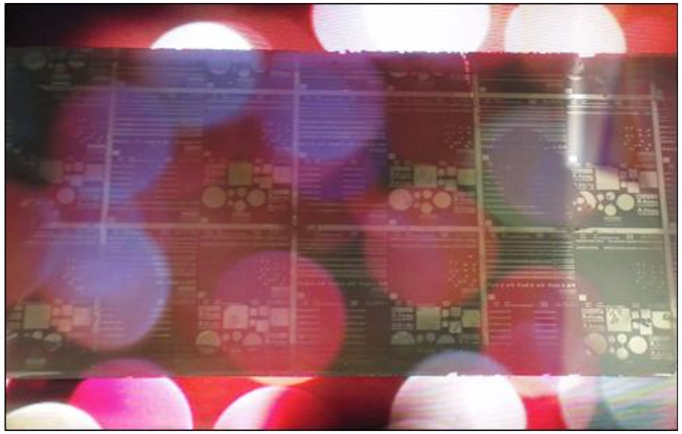


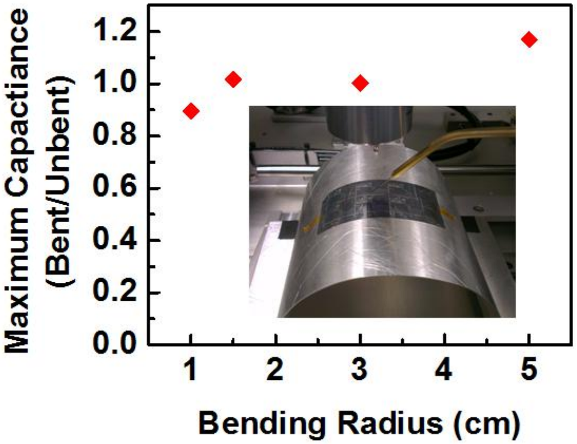
- ☐ ***Deployment of advanced high-k/metal gate stacks for LSTP applications***
- ☐ ***10,000 devices were fabricated***

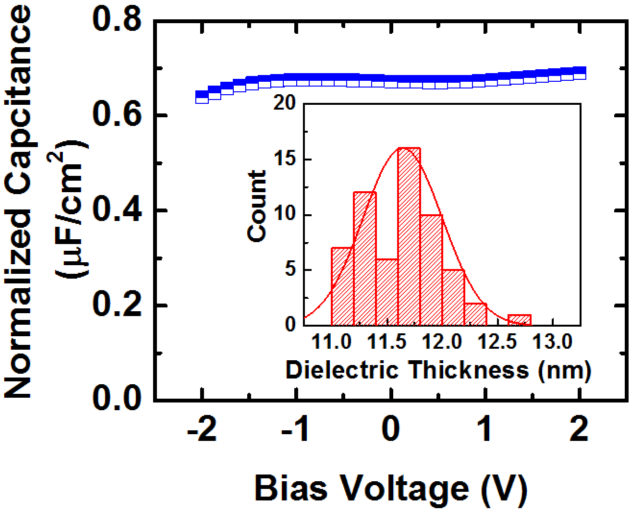
J. P. Rojas, M. M. Hussain (pss-RRL 2013)

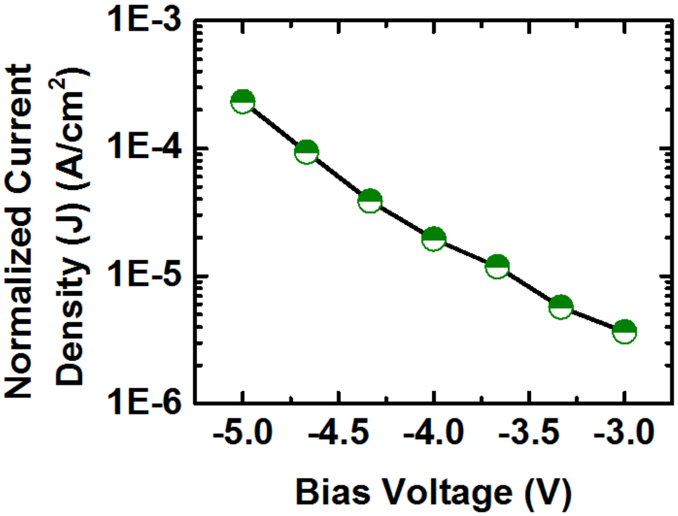
High-κ/metal gate MIMCAPs for DRAM







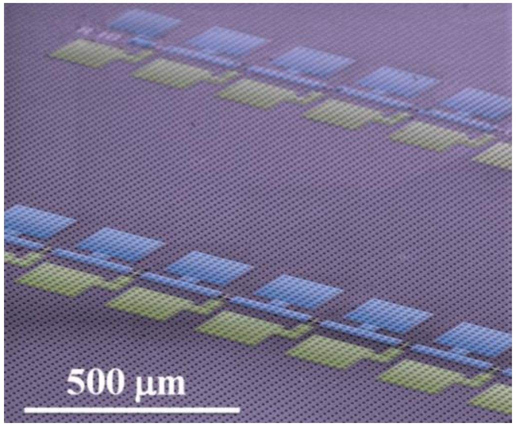


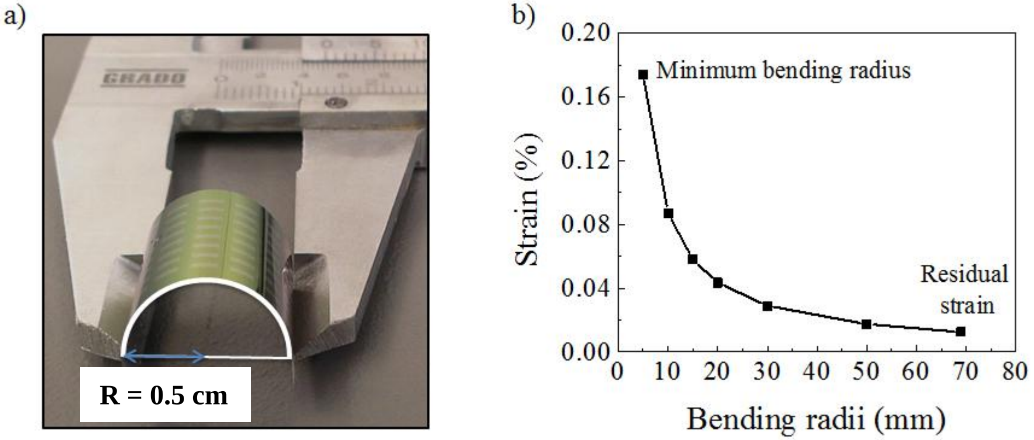


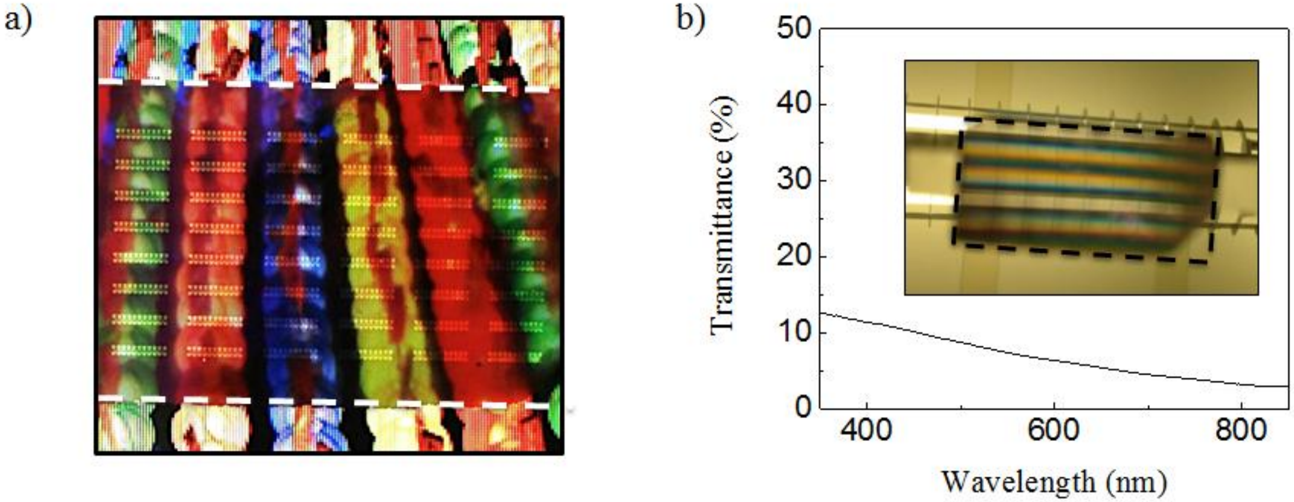
- ☐ ***DRAM is an integral component***
- ☐ ***High aspect ratio complex feature***

J. P. Rojas, M. T. Ghoneim, C. Young, M. M. Hussain (IEEE TED 2013)

High-κ/metal gate MOSFETs for SRAM



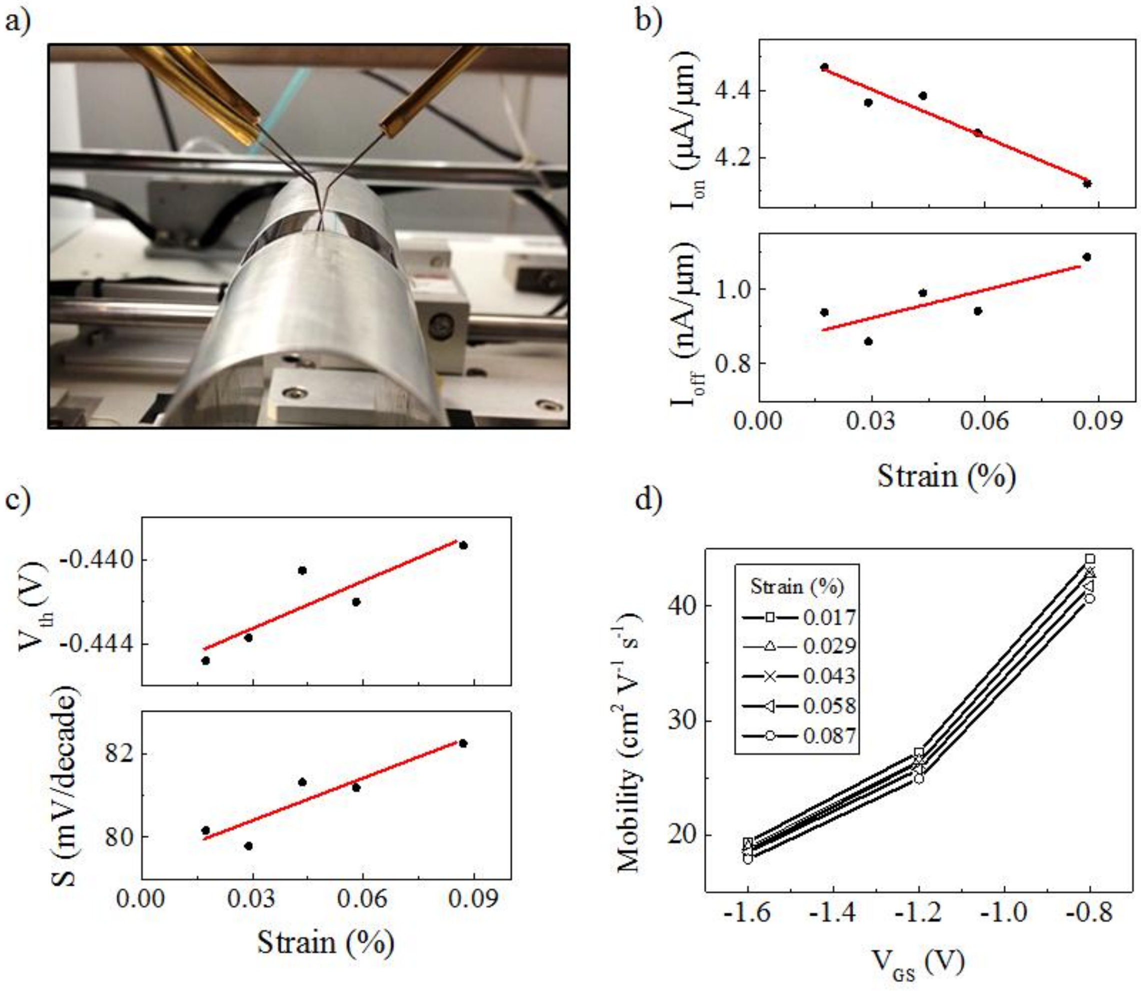




- ***PMOS – large devices***
- ***Bending radius getting reduced***
- ***Further improvement is possible***
- ***Transmittance quantified***

J. P. Rojas, G. A. Torres Sevilla, M. M. Hussain (Pending Review)

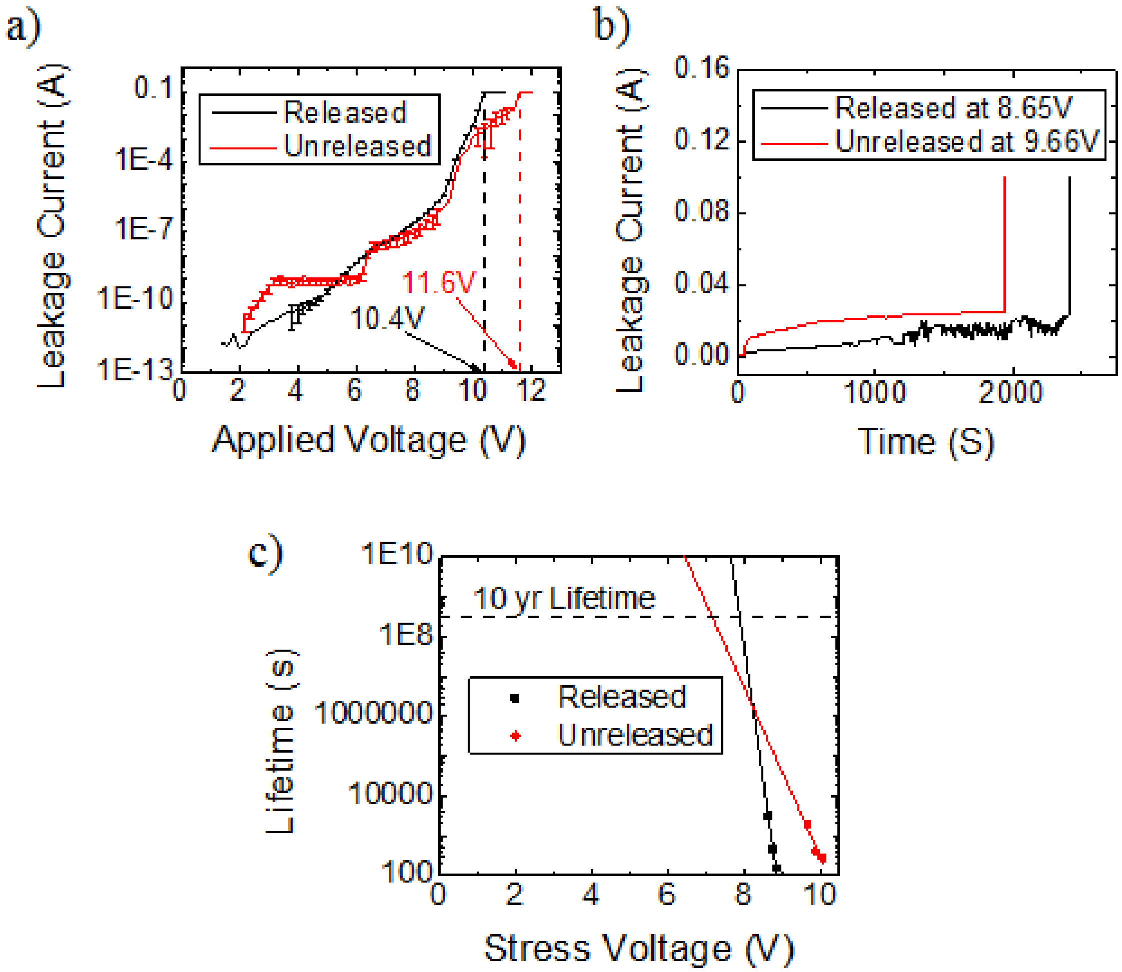
Performance while bent



- ***Insignificant performance variation while bent***
- ***Extensive measurements need to be performed while bent***
- ***Need more advanced standardized tools than custom made toolsets***

J. P. Rojas, G. A. Torres Sevilla, M. M. Hussain (Pending Review)

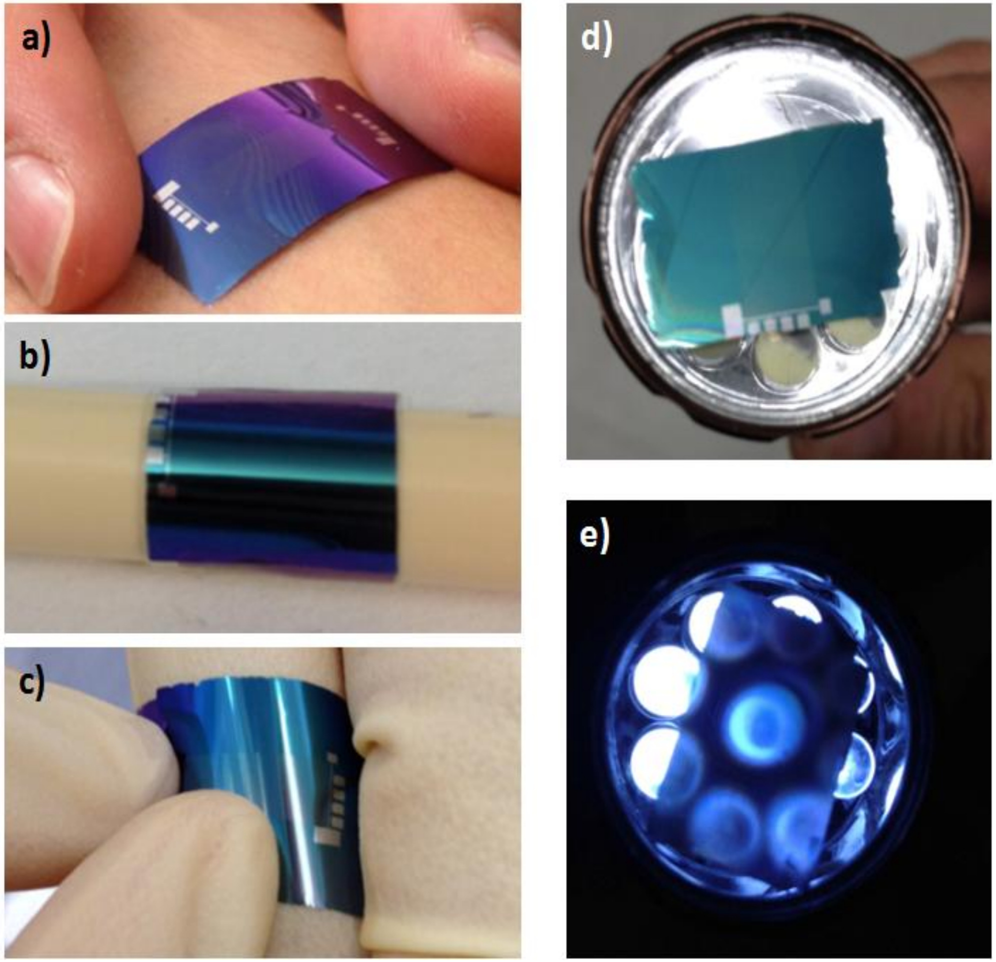
Reliability analysis

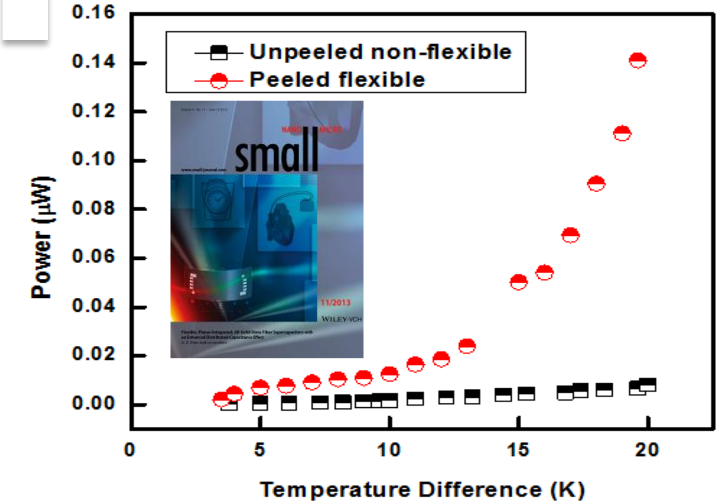


- ***Reliability analysis is an important metric in semiconductor industry***
- ***TDDB, charge pumping, BTI, SILC***
- ***Still making progress to understand the actual impact of process and overall flexibility***

J. P. Rojas, M. T. Ghoneim, C. Young, M. M. Hussain (Pending Review)

Moving towards electronic systems





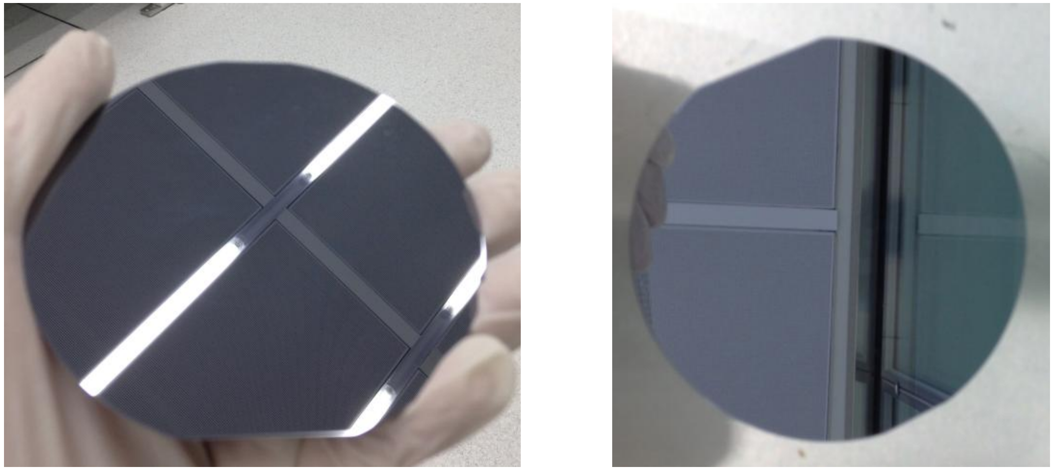
- ***Flexible thermoelectric generator***
- ***3.6% thickness of bulk silicon***
- ***Reducing thermal loss***
- ***Increasing output power by 30%***

G. Torres Sevilla, S. Inayat, A. Hussain, J. P. Rojas, M. M. Hussain (Small 2013)

Recyclability

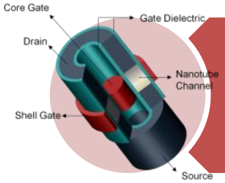
- To release 25 μm Si fabric, we consume 75 μm of bulk Si
- We have recycled the remaining wafer by CMP
  - A standard wafer (0.5 mm thickness) has been recycled 6 times
  - Extreme care and precision tools are required for the last wafer(s)
- This way we generate 6 silicon fabric from 1 wafer
- Our current process causes 16% area loss

VIDEO0007.mp4

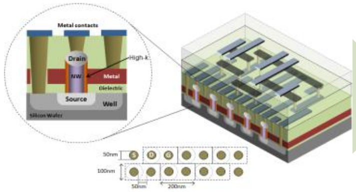


G. Torres Sevilla, S. Inayat, S. Ahmed, A. Hussain, J. P. Rojas, M. M. Hussain (Transducers 2013)

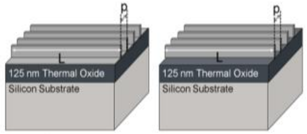
Proponents for smart living



High performance mobile computation with longer battery lifetime



Multi-functionality (ULSI)



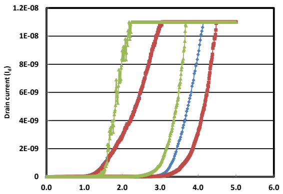
$S_{WCFET} \propto (A_{WCFET})^{-3/2} \propto {}^{1}/{(RC)_{WCFET}}$

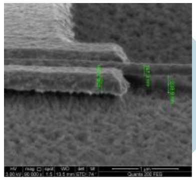
$P_{WCFET} \propto C_{WCFET}V^2$

$S_{FinFET} \propto (A_{FinFET})^{-3/2} \propto {}^{1}/{(RC)_{FinFET}}$

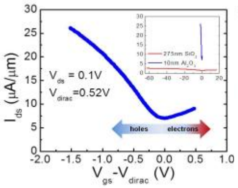
$P_{FinFET} \propto C_{FinFET}V^2$

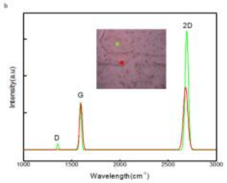
High resolution display



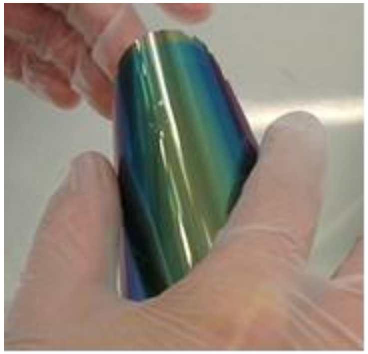


Multi-tasking





High speed communication

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rapid research letters

3

2013

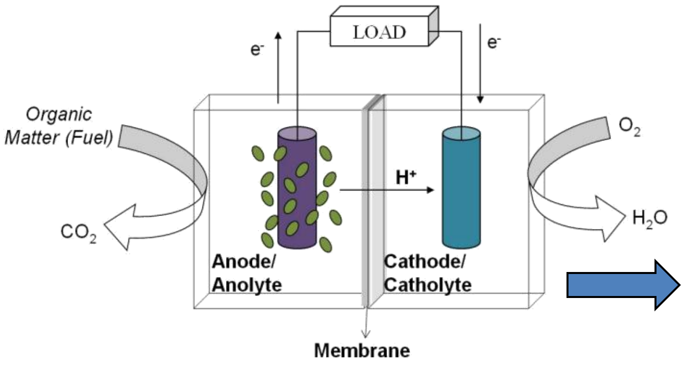
Flexible semi-transparent silicon (100) fabric with high-k/metal gate devices

Jhonathan P. Rojas and Muhammad Mustafa Hussain

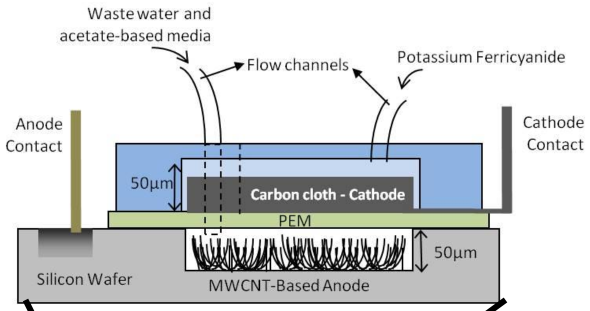
WILEY-VCH

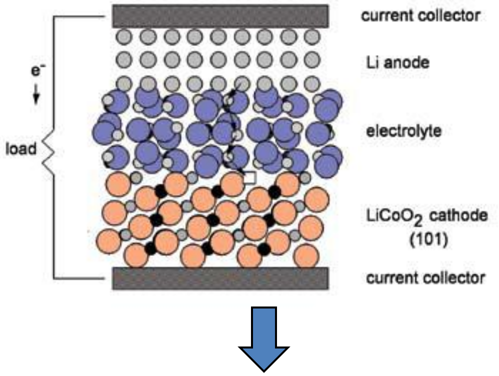
Conveniently powered: energy chip to power card

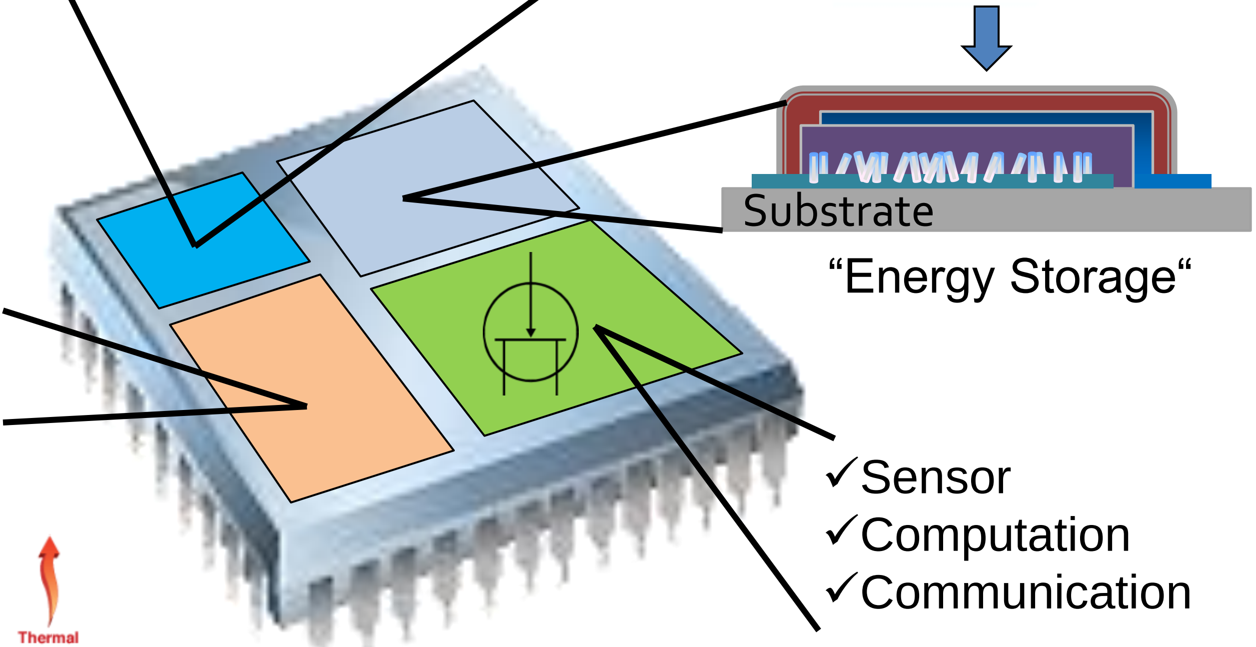
Card size rechargeable low cost and weight thin battery



"Microbial Fuel Cell"



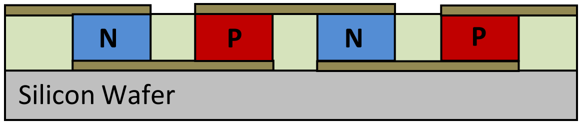


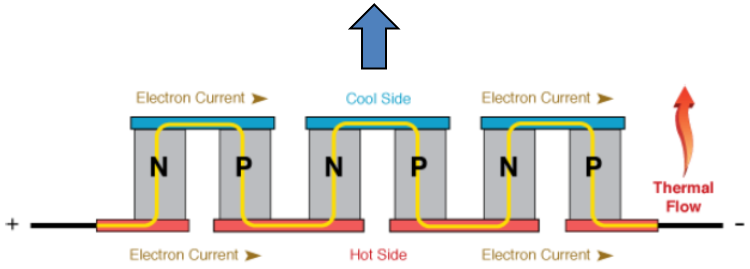


"Energy Storage"

- ✓Sensor
- ✓Computation
- ✓Communication

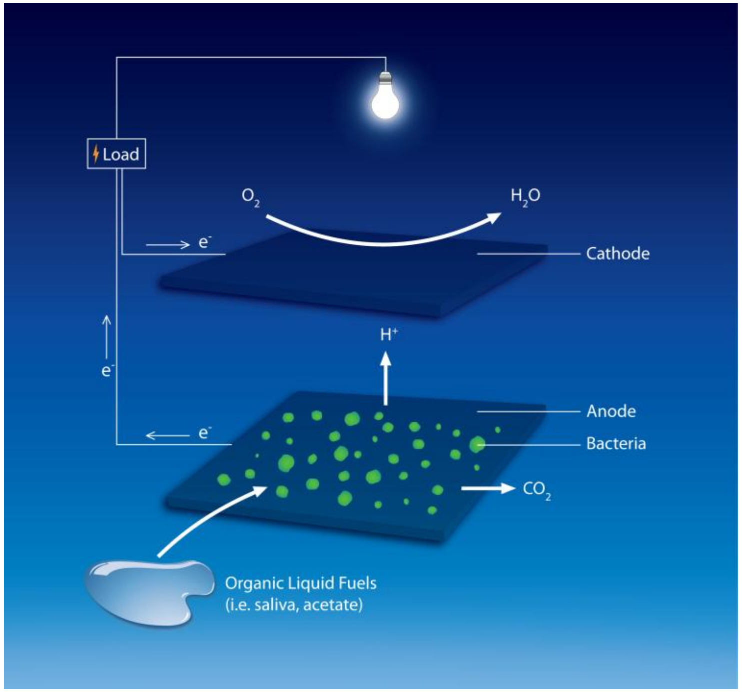
"Thermoelectric Generator"

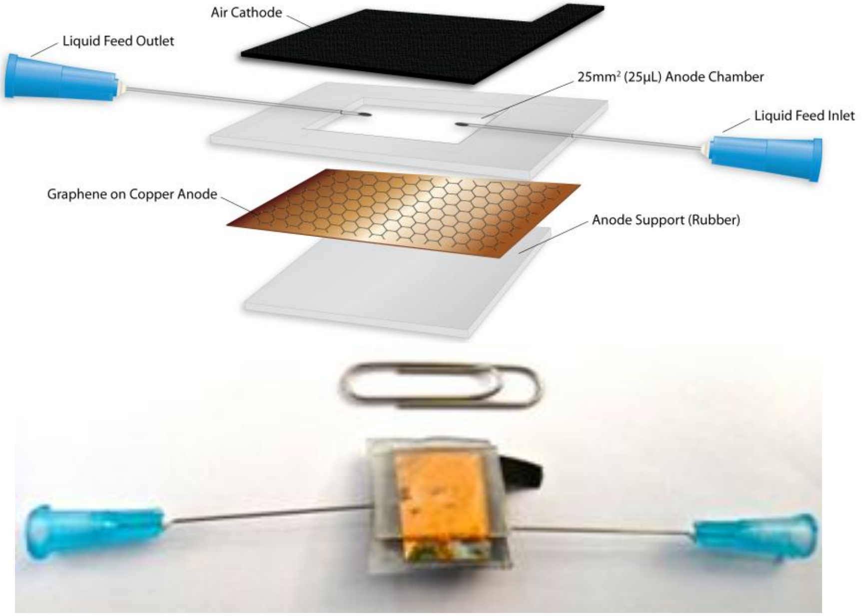




Microbial fuel cell

- All the existing and known technologies for water desalination and purification consume massive amount of energy
- Exception is microbial fuel cell (MFC) which harnesses the electricity generated through the metabolic processes of electrogenic bacteria when decomposing organic matter



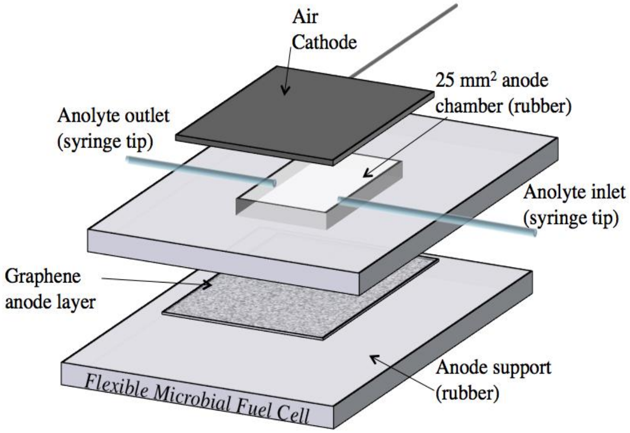


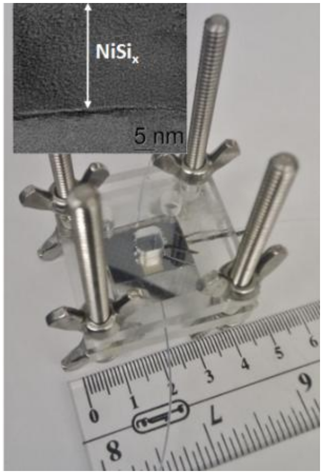
http://nanotechnology.kaust.edu.sa

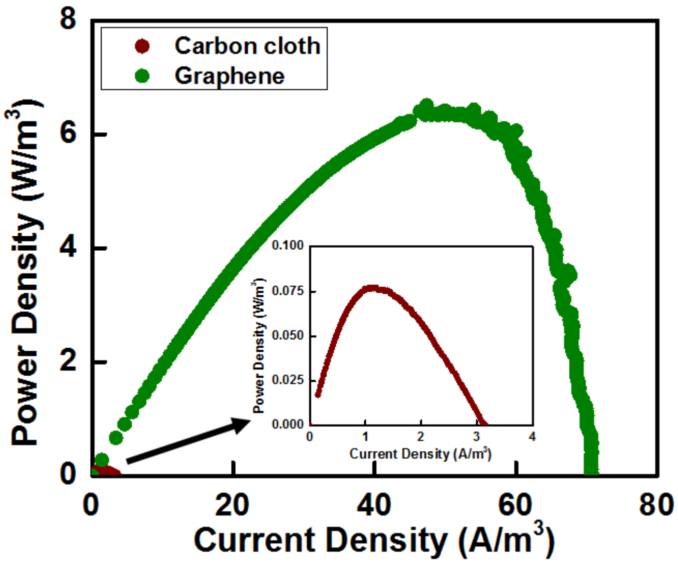
Micro-sized microbial fuel cell

- Macro-version of MFC takes months to carry out one experiment – lingering its development for practical applications
  - A micro-sized MFC can provide a result in weeks
- We used silicon and conventional micro-fabrication processes for rapid prototyping at an affordable cost to expedite R&D
  - Integrated carbon based nano-materials:
    - Multi-walled carbon nanotube and graphene as anode
  - Integrated metal silicide to reduce contact resistance for higher output current
    - Nickel, aluminum, titanium and cobalt-based silicides
  - Used low-cost rubber as flexible host platform
  - Used air cathode to eliminate continuous feeding for more sustainable design
  - Even saliva can be used as fuel …!

Fabrication of micro-sized MFC

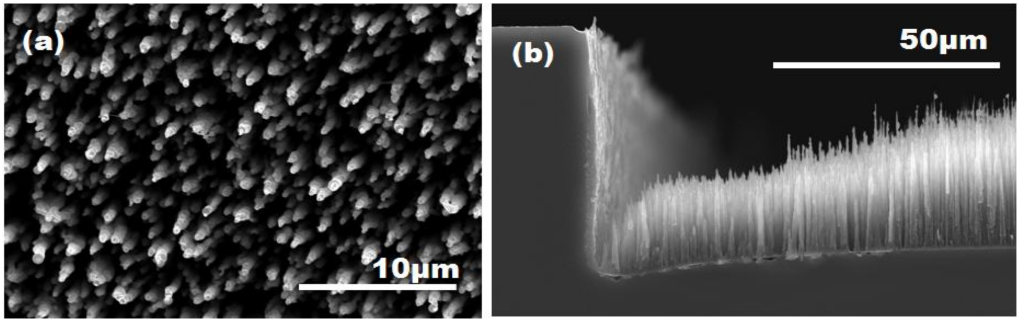


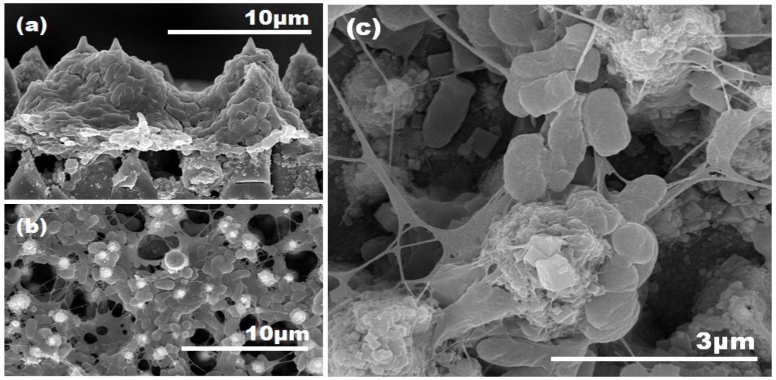




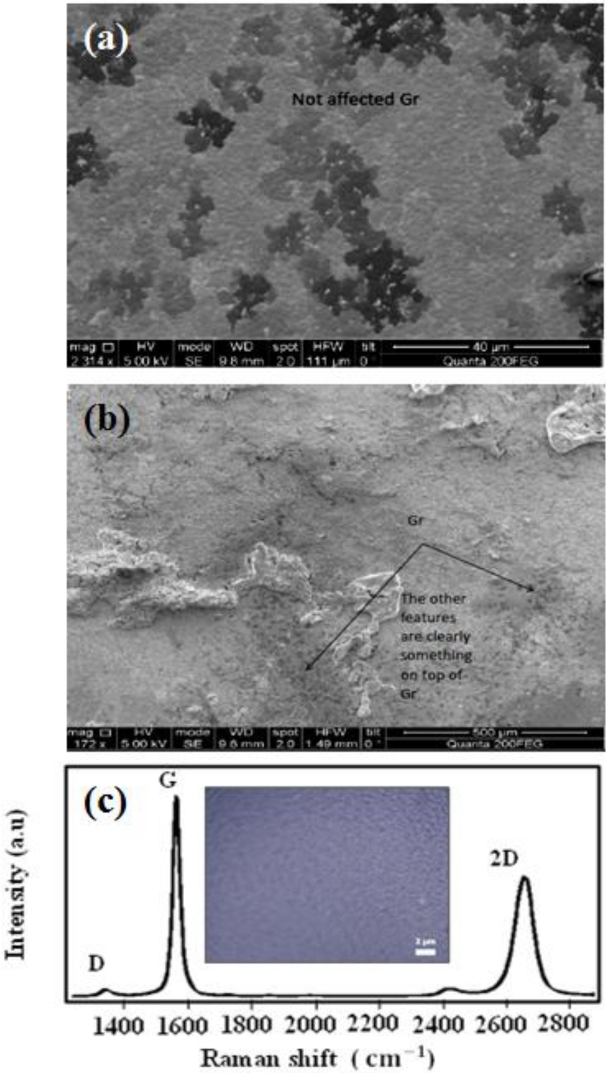
- Silicon has been used as base substrate
- One step photolithography, etch and metallization has been performed using Physical Vapor Deposition
- Chemical vapor deposition based CNT and graphene has been grown
- Metal deposition followed by annealing has been done for salicidation (salicidation provides *Ohmic contact*)
- Special care has been taken during assembly

Biocompatibility of nano-materials

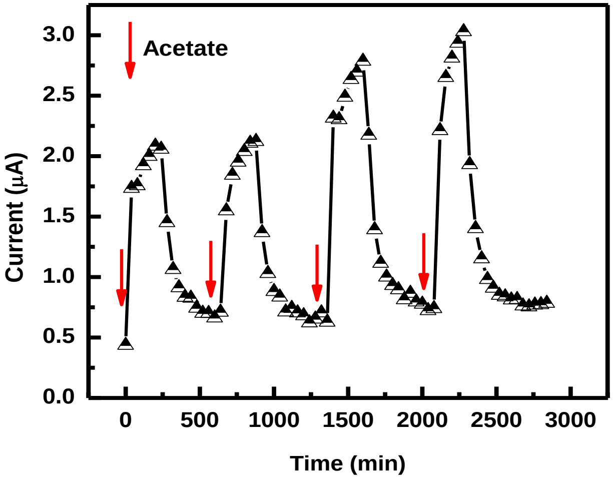




CVD grown high quality MWCNT (1D material system) and multi-layer graphene (2D atomic crystal structure material) show desired bacterial growth ➔ biocompatibility

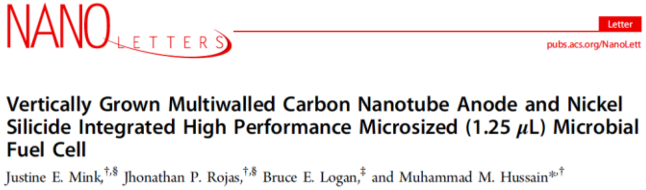


High performance from tiny devices



Anode			Cathode		P_{Max}	P_{Max}	$I_{max\,@\,Pmax}$	$I_{max\,@\,Pmax}$	Ref.
V (µl)	Material (cm^2)	Inoculum/ Fuel	Material	Solution	(mW/m²)	(W/m³)	(mA/m²)	(A/m³)	
1.25	**MWCNT (0.25)**	***Mixed bacterial culture/ Acetate***	**Carbon Cloth**	**$[Fe(CN)_6]^{3-}$**	**19.6**	**392**	**197**	**3947**	**Mink**
1.5	Gold (0.15)	*Shewanella putrefacien/* Lactate	Carbon Cloth	$[Fe(CN)_6]^{3-}$	1.5	15.3	130	1300	Qian
4.5	Gold (2.25)	*Geobacteraceae-* enriched/ Acetate+ L-Cysteine	Gold	$[Fe(CN)_6]^{3-}$	47	2300	116	5777	Choi
15	Gold (2.16)	*Saccharomyces-cerevisiae/* Glucose	Gold	$[Fe(CN)_6]^{3-}$	4	32.1	167	2400	Siu

- ☐ Rapid performance analysis is possible using micro-sized MFC
- ☐ High surface-to-volume ratio 1D and 2D materials plus improved contact resistance contribute to high performance ➔ pragmatic step towards self-powered devices

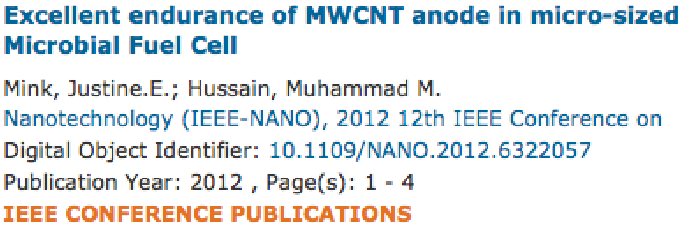

NANO LETTERS Letter
pubs.acs.org/NanoLett

Vertically Grown Multiwalled Carbon Nanotube Anode and Nickel Silicide Integrated High Performance Microsized (1.25 µL) Microbial Fuel Cell

Justine E. Mink,[†,§] Jhonathan P. Rojas,[†,§] Bruce E. Logan,[‡] and Muhammad M. Hussain[*,†]

2012 MRS FALL MEETING

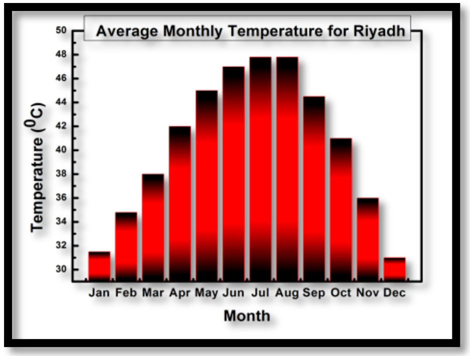
IEEE NANO

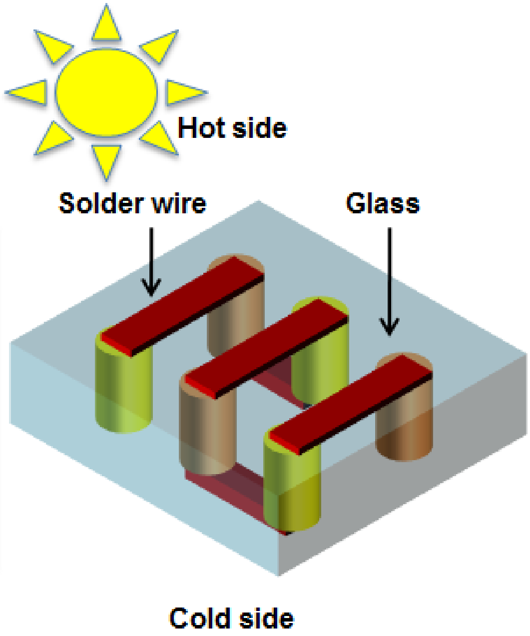

Excellent endurance of MWCNT anode in micro-sized Microbial Fuel Cell

Mink, Justine.E.; Hussain, Muhammad M.
Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on
Digital Object Identifier: 10.1109/NANO.2012.6322057
Publication Year: 2012 , Page(s): 1 - 4
IEEE CONFERENCE PUBLICATIONS

Thermoelectric windows

- Objective: Harness clean thermoelectric energy from the naturally existing temperature difference between the hot outside and cold inside of a building in a hot weather area (Middle East, Sub-Sahara)
- We enjoy appreciable temp. difference in Saudi Arabia
- Rapid urbanization offers many high rise buildings with large area glass window





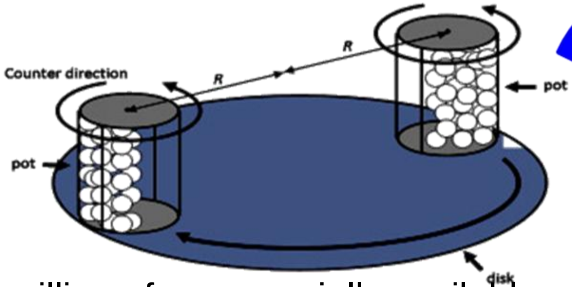
- Global status-quo: Research on thermoelectric materials with improved ZT factor, but not on systems. $ZT = \left(\frac{\sigma S^2}{k}\right) T$
  - σ = Electrical conductivity
  - S = Seebeck coefficient
  - *k* = Thermal conductivity
  - T = Temperature difference

Difficult to find a material system whose electrical conductivity is high but thermal conductivity is low

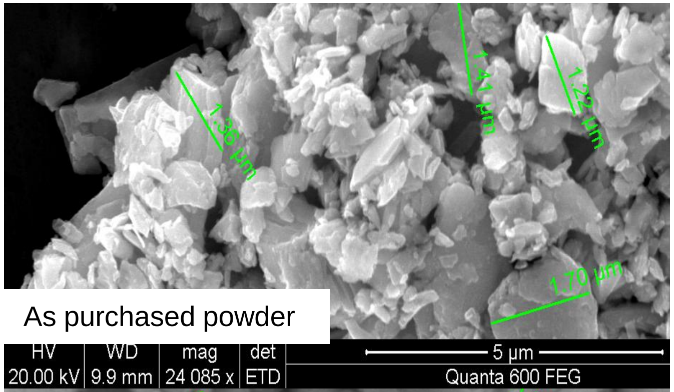
A typical window glass is >5 mm thick – no known technique can provide such thick thermoelectric material(s) specially through an interface

Scientific and engineering approach

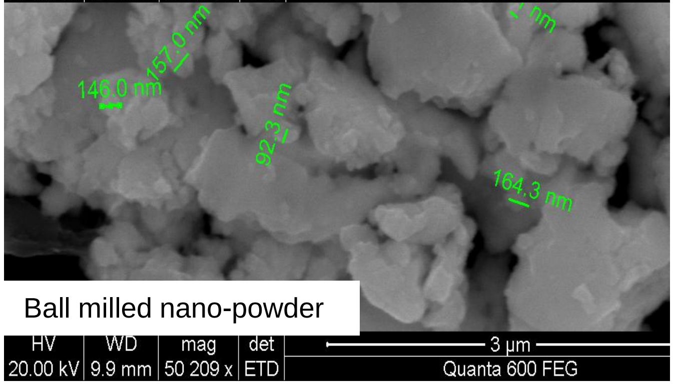
- Electrochemical deposition or conventional micro-fabrication techniques (such as evaporation or sputtering) are not usable for thick thermoelectric materials fabrication which will be embedded through interface



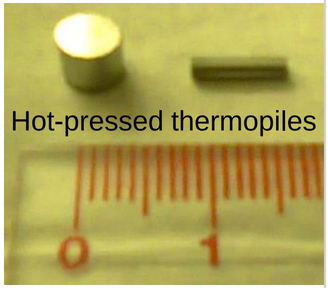
Ball milling of commercially available thermoelectric material in powder format



As purchased powder



Ball milled nano-powder

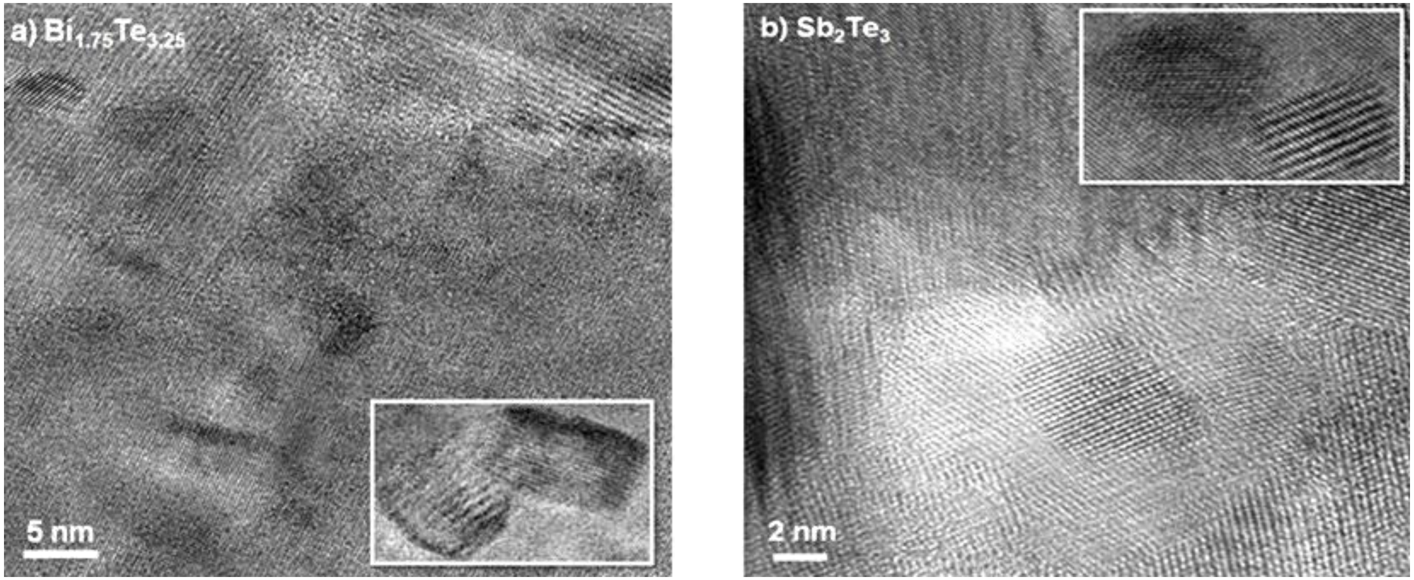


Hot-pressed thermopiles

Hot pressing to make 5 mm long thermopiles using thermoelectric nano-materials

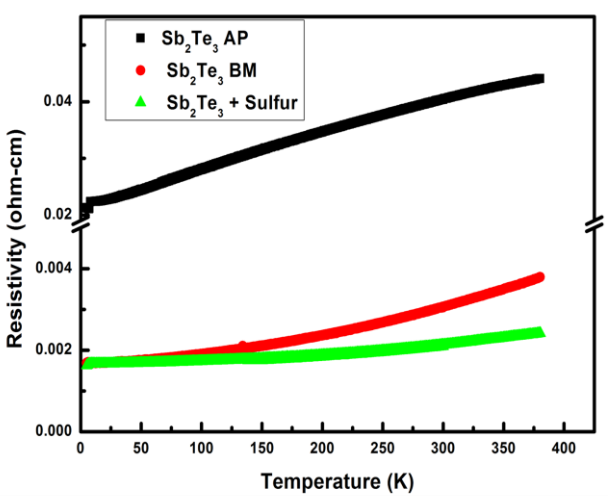
Applied Nanoscience, 2012, DOI: 10.1007/s13204-012-0139-z

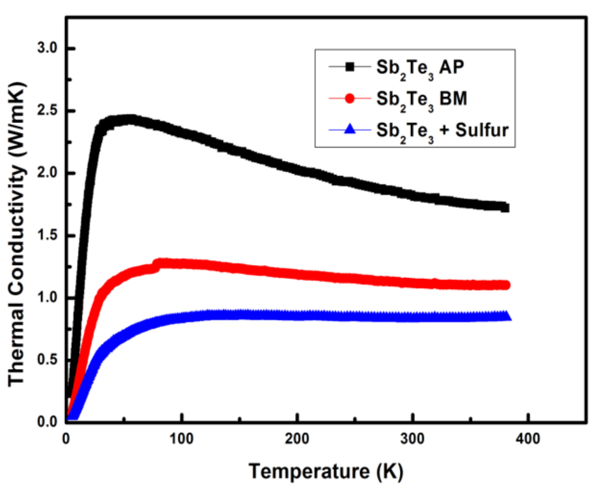
Impact of nano-structuring

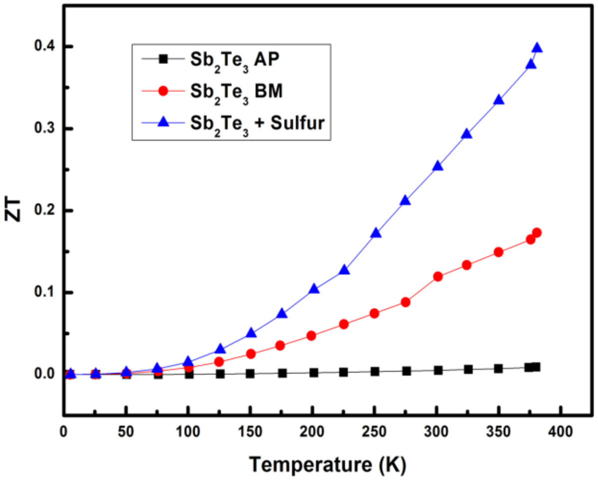


- Confirmed nano-structuring by TEM analysis
- Bismuth telluride (Bi_2Te_3) with angular boundaries ➔ pronounced boundary scattering
- Antimony telluride (Sb_2Te_3) with circular boundaries ➔ lesser phonon scattering

Sulfur modulated thermoelectric property improvement



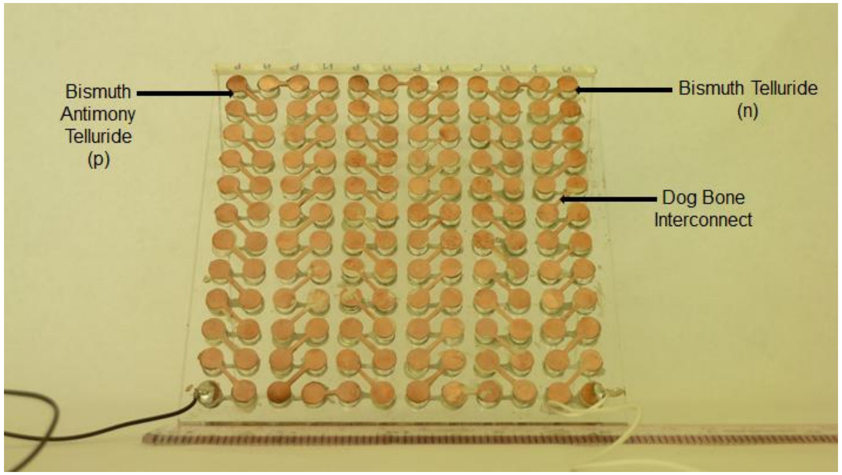


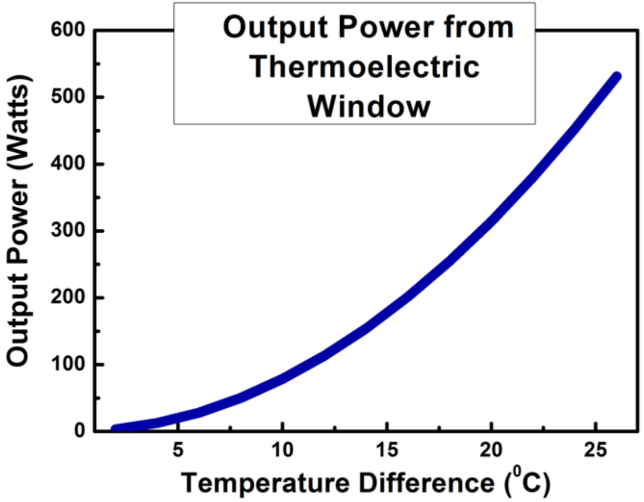


- Sulfur addition suppresses carrier concentration ➔ higher Seebeck coefficient, lower thermal conductivity
- It also causes potential barrier scattering of carriers due to enhanced micro structural refinement ➔ higher ZT

__Scientific Reports (Nature Publishing Group)__, DOI: 10.1038/srep00841

Integrated thermoelectric systems





- 72 pairs of thermopiles embedded thermoelectric systems demonstrated on real window glass
- At a temperature difference of 20 °C, from a 9 m^2 window glass, 310 watts of power is achievable
- Improved contact engineering can significantly improve performance
- Comparable transparency with designed window glass

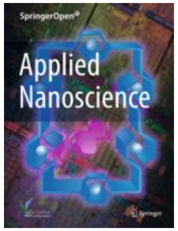
SCIENTIFIC REPORTS

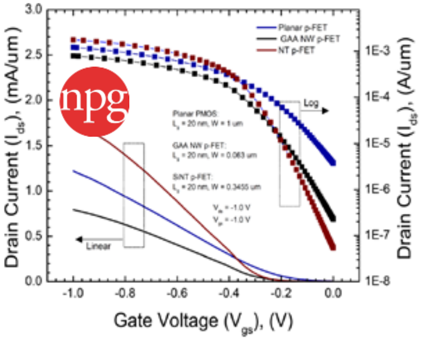
2012 MRS FALL MEETING

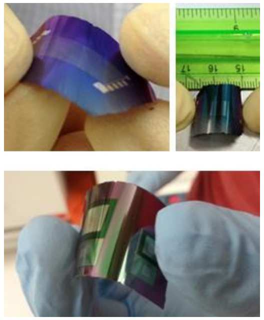
International Conference on Thermoelectrics ICT/ECT JULY 9TH-12TH 2012 AALBORG DENMARK

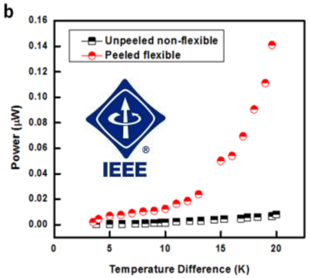
2012 Asia Pacific Clean Energy Summit and Expo

ISCA Dow Sustainability Innovation Student Challenge Award

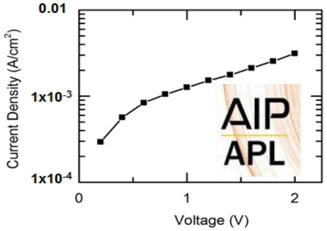


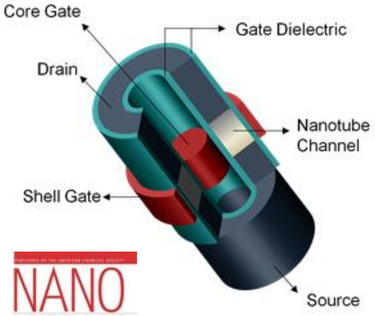






SPIE Defense, Security+Sensing





NANO LETTERS

Si, II-IV, III-V Nanotube Architecture Devices

For high performance computation at ultra low power, sensors, displays and energy applications

Flexible Inorganic Electronics

For ultra mobile computation, in-vivo/vitro medical electronics, widely deployed sensors and energy applications

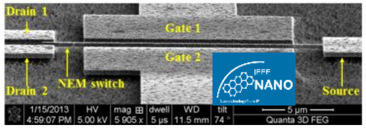
Integrated Nanotechnology for Smart Living and Sustainable Future

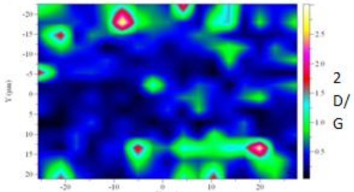
Energy Chip and Power Card

For ultra-mobile and self-powered electronics

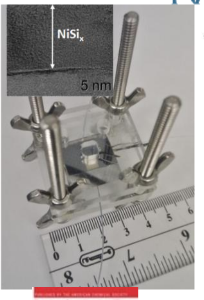
Thermoelectric Windows

For mass-scale thermoelectricity for energy efficient buildings

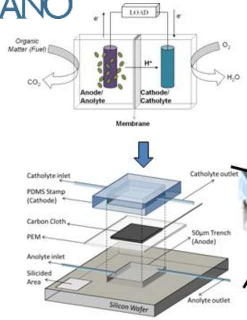


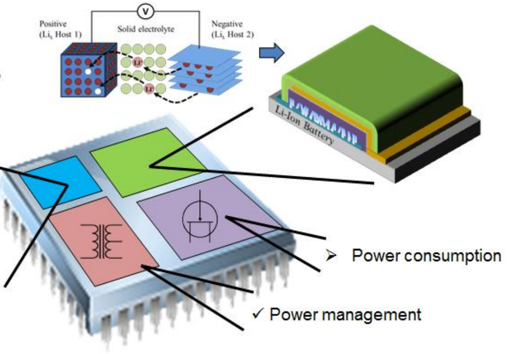


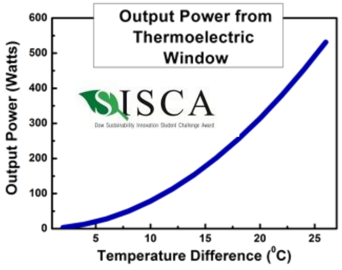
ACS NANO

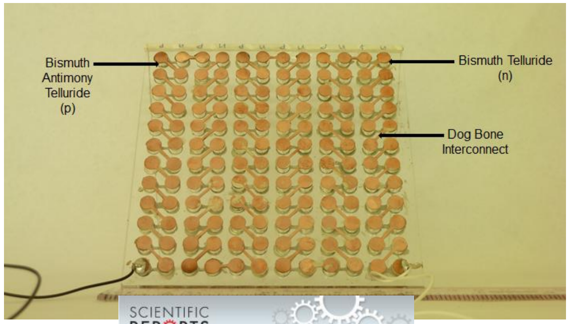


NANO LETTERS



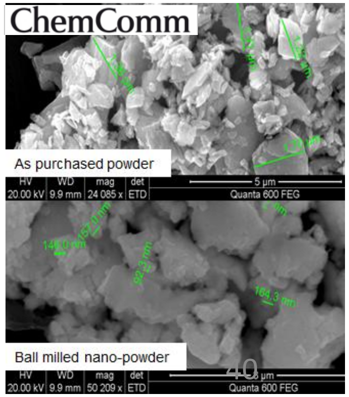






SCIENTIFIC REPORTS

ChemComm



INTEGRATED NANOTECHNOLOGY LAB @ KAUST

Principal Investigator: Dr. Muhammad Mustafa Hussain, Electrical Engineering
http://nanotechnology.kaust.edu.sa

From left to right (back row): MMH (Bangladesh-USA), Amir (Egypt), Galo (Ecuador), Ramy (Saudi Arabia), Casey (USA), Aftab (India), Fahad (Bangladesh), Jhonathan (Colombia), Ghoneim (Egypt)
From left to right (front row): Maha (Saudi Arabia), Joanna (Lebanon), Sally (Egypt), Justine (USA), Kelly (USA)
Not present: Salman (Pakistan), Abdulilah, Eman, Amal, Bidoor, Rabab, Arwa (Saudi Arabia)